A Novel Quaternary Half Subtractor Using 2:1 Multiplexer

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Abstract: - Multiple-valued logic (MVL) is a logic in which there are more than two truth values. MVL is used due to difficulty in interconnection problems in binary system. Carbon nanotube field-effect transistors (CNTFET) is used to design the Quaternary Half Subtractor (QHS) circuit. Sub blocks of Module (0210), Module (1021), Module (2102), Module (3210) using three supply voltage devices and Quaternary Multiplexer 2:1 using pass transistor have designed in this paper. Therefore, compared to existing designs, less no. of transistors are needed. Comparing proposed Half subtractor using 4:1 MUX modules to current one's reveals that the 2:1 multiplexer-based method leads in lower power usage. These proposed designs have proven to work satisfactorily under a variety of operating situations, including power, delay, and power delay product (PDP).

Key-Words: - Half Subtractor, CNTFET, quaternary logic, 2:1 multiplexer, 4:1 multiplexer, Transmission gate logic, Pass Transistor Logic

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1. Introduction

Multi-valued logic (MVL) goes beyond the traditional binary system by using more than two logic states. Compared to binary circuits, MVL circuits can offer significant advantages. By increasing the number of possible logic values, MVL enables higher storage densities, allowing more data to be stored with fewer connections. This reduction in connections can lead to lower power consumption and a smaller chip area. As a result, MVL circuits have the potential to process and store more data efficiently, which is crucial for optimizing modern electronic systems [1].

A newer type of multi-valued logic (MVL), known as quaternary logic, uses four distinct logic levels. When implemented using conventional complementary metal oxide semiconductor (CMOS) technology, quaternary logic circuits rely on multiple thresholds, which can be achieved through body biasing of MOS transistors [2]. However, scaling CMOS technology to the nanoscale introduces challenges such as short-channel effects, reduced gate control, increased power dissipation, and greater variability in device structure and doping, all of which can negatively impact performance [3].

We addressed this issue using CNTFET (Carbon Nanotube Field-Effect Transistor) technology. CNTFETs offer several advantages, including better control over channel formation, high electron density, enhanced transconductance, and increased current capacity [4]. One of the key benefits of CNTFETs is the strong correlation between the threshold voltage and the nanotube diameter [5]. The most promising CNTFET design is a MOSFET-like structure, incorporating both p-type and n-type transistors.

The inverse relationship between nanotube diameter and threshold voltage allows for easy adjustment of CNTFET threshold voltages. This is a significant advantage over CMOS, which requires multiple masks to achieve different threshold voltages. As a result, designing multi-level circuits becomes simpler and more efficient. In recent years, numerous researchers have developed MVL circuits using CNTFET technology [6].

2. Background

2.1 CNTFET-Based Quaternary Logic

A quaternary logic function consists of four values: 0, 1, 2, and 3, which correspond to voltage levels of 0, one third VDD, two third VDD, and VDD, respectively. This research utilizes three types of quaternary inverters: positive quaternary inverter (PQI)[7], intermediate quaternary inverter (IQI)[7], and negative quaternary inverter (NQI)[7]. The characteristic equations for each of these four-level inverters are presented in Equations (1, 2, 3). Table 1 provides the definitions of the quaternary inverters commonly used in quaternary logic.

$$NQI = \begin{cases} 3 & if\ IN = 0 \\ 0 & if\ IN \neq 0 \end{cases} \quad (1)$$

$$IQI = \begin{cases} 3 & if\ IN = 0\ or\ 1 \\ 0 & if\ IN = 2\ or\ 3 \end{cases} \quad (2)$$

$$PQI = \begin{cases} 3 & if\ IN \neq 3 \\ 0 & if\ IN = 3 \end{cases} \quad (3)$$

Table 1 [7] Quaternary Inverters

INPUT	NQI	IQI	PQI	SQI
0	3	3	3	3
1	0	3	3	2
2	0	0	3	1
3	0	0	0	0

The integration of CNTFET technology in MVL circuit design has enabled the development of quaternary circuits, such as the Low Power Quaternary Adder Using CNFET [8-9], Area Optimized and Energy Efficient Quaternary Circuits [10], Quaternary Digital Circuits [11-12], a Quaternary Full Adders [13-14] and a Quaternary Multipliers [15-16]. Each of these designs incorporates quaternary multiplexers, which are implemented using transmission gate logic.

3. Proposed Half Subtractor Module

3.1 Proposed Quaternary Half Subtractor using 4:1 MUX (QHS)

In Fig.2(a), the output of Multiplexer is (Module (0210)) When A='0', while A='1', the output of Multiplexer will be equivalent to (Module (1021), when A='2', then it results as output of Multiplexer is (Module (2102), and when A='3', the output of Multiplexer is equal to (Module (3210), based on the quaternary half Subtractor (QHS) truth table (Table 2).

Table 2 Truth Table for QHS

A	B	Difference	Borrow
0	0	0	0
0	1	2	1
0	2	1	1
0	3	0	1
1	0	1	0
1	1	0	0
1	2	2	1
1	3	1	1
2	0	2	0
2	1	1	0
2	2	0	0
2	3	2	1
3	0	3	0
3	1	2	0
3	2	1	0
3	3	0	0

In Fig.2(b), Borrow is equal to $\overline{(NQI(B))}$, only when we pass input as A='0', when A='1', then Borrow is similar to $\overline{IQI(B)}$, when A='2', then Borrow is equal to $\overline{PQI(B)}$, when A='3', then Borrow is exactly '0'.Figure 2 depicts the block diagram for constructing the proposed quaternary half Subtractor (Difference and Borrow -QHS) and truth table of Quaternary Half Subtractor is shown in Table 2.

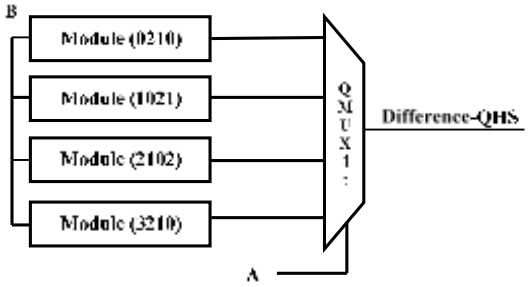

Fig. 1. Diagram of the Difference-QHS

3.2. Existing Quaternary Multiplexer 4:1

Figure 3 shows the 4:1 quaternary multiplexer [7] function.

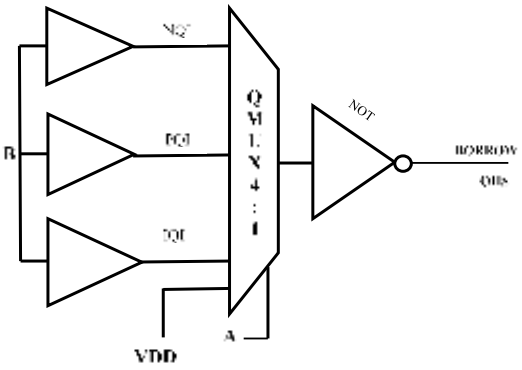

Fig. 2. Diagram of the Borrow-QHS

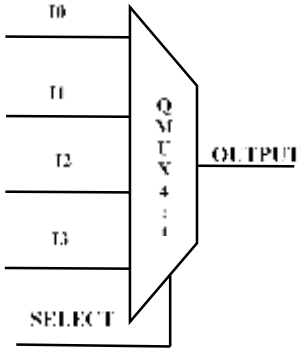

Fig.3(a). Symbol of the 4:1 Quaternary MUX[7]

3.3 Sub Modules of QHS

The Proposed Module (0210), Module (1021), Module (2102), Module (3210) operations are discussed. Modules (0210), (1021), (2102), and (3210) are designed in a three-supply voltage configuration in this work. Four supply voltages used for logic 3, 2, 1, 0 are VDD, 2VDD/3, VDD/3 and 0 V respectively.

The operation of Module (0210), depends on the selection signal B = 0 to 3, for which outputs are 0, 2VDD/3, Vdd/3 and 0 respectively. which is shown in Fig 4(a).

The operation of Module (1021), shown in Fig. 4(b), is also follows the logics 1, 0, 2, 1 based on B. Similarly, module (2102), Fig 4(c) also gives output as per the logic 2, 1, 0, and 2 based on B. Fig 4(d) produces output 3, 2, 1, 0 which is called Module (3210).

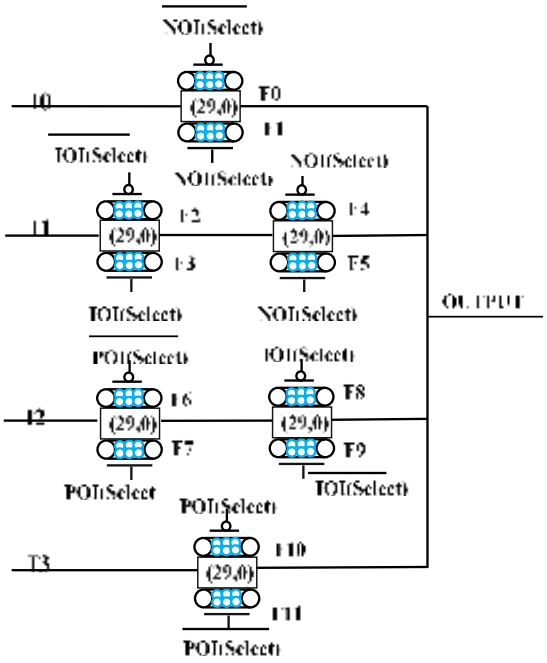

Fig. 3(b). Design of the Existing Quaternary Multiplexer 4:1[7]

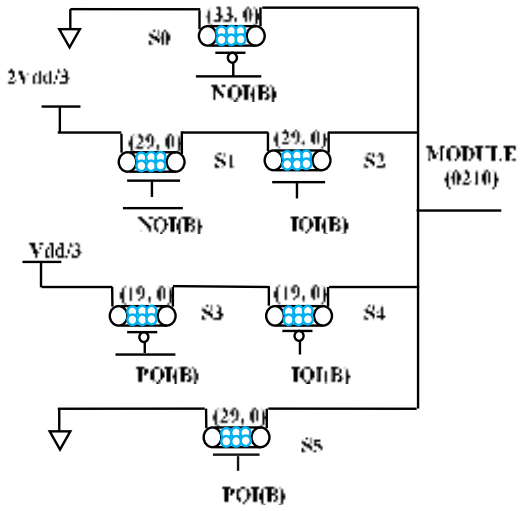

Fig .4(a). Proposed Module (0210)

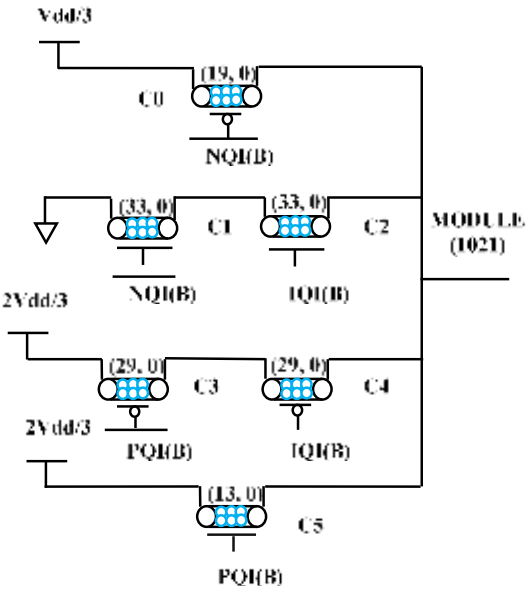

Fig.4(b). Proposed Module (1021)

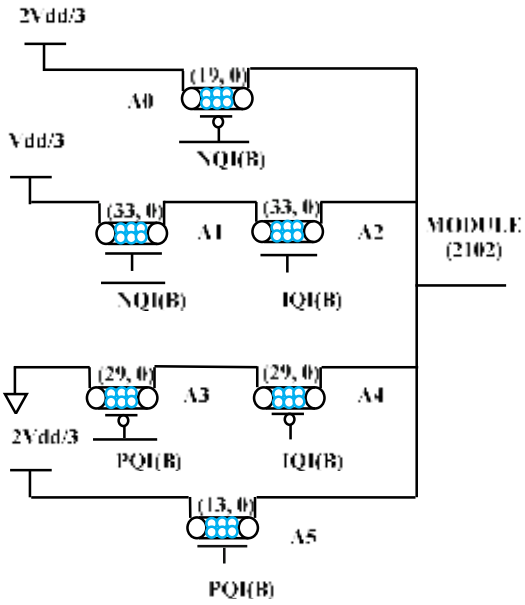

Fig.4(c). Proposed Module (2102)

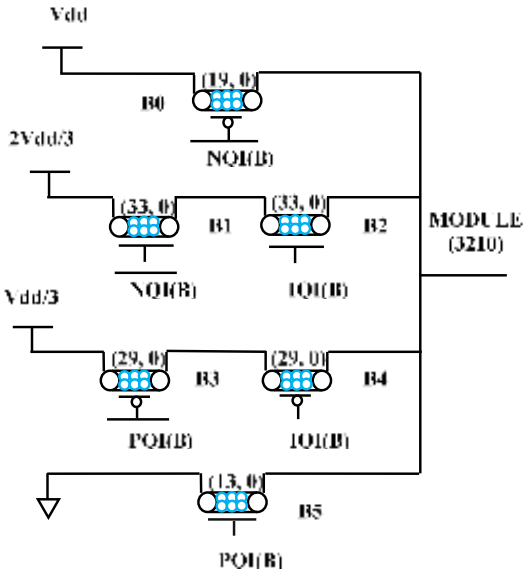

Fig.4(d). Proposed Module (3210)

4. Proposed Quaternary Half Subtractor Using 2:1 Mux (QHS)

To reduce the number of transistors in the existing quaternary circuit, specifically the Quaternary Half Subtractor (QHS) shown in Figure 4 using a 4:1 multiplexer (MUX), we propose a new design for the Quaternary Half Subtractor (QHS) using a 2:1 MUX, as shown in Figure 5.

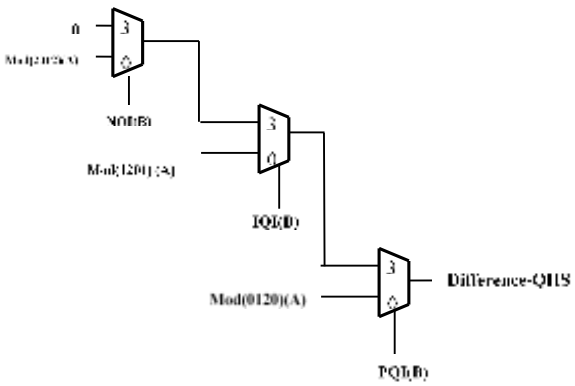

Fig.5(a). Proposed design for quaternary Difference -QHS using 2:1 MUX

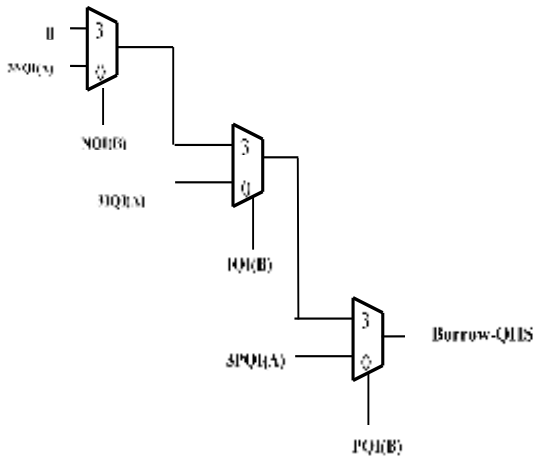

Fig.5(b). Proposed design for Quaternary Borrow-QHS using 2:1 MUX

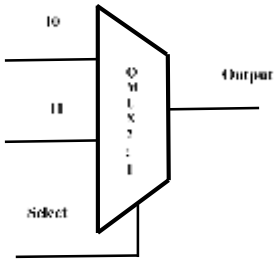

Fig. 6(a). Symbol of the Existing 2:1 Quaternary MUX[7]

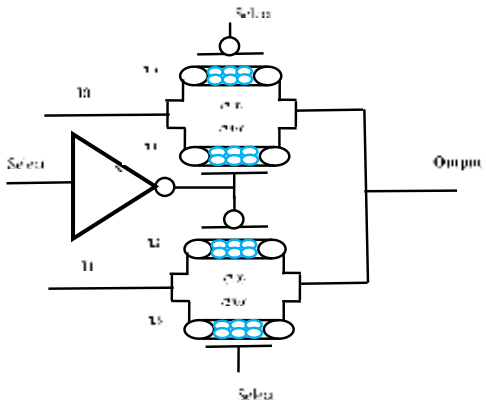

Fig .6(b). Design of the Existing Quaternary Multiplexer 2:1[7]

Figure 6 demonstrates the operation of the current 2:1 Quaternary Multiplexer. In the first section, the output is 3 when the select input is "0" and the NQI input is 0. When the select input is "0," transistors T0, T1, and T2 are ON, while transistors T2 and T3 are OFF, allowing the input I0 to pass to the output based on the threshold voltage and type of transistors used. The existing 2:1 Quaternary Multiplexer is illustrated in Fig. 6.

4.1 Sub Modules of Borrow Generation

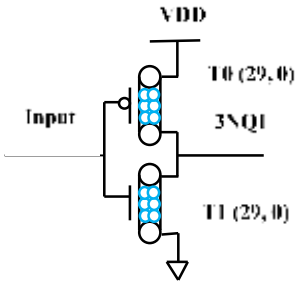

Fig .7(a) Proposed 3NQI

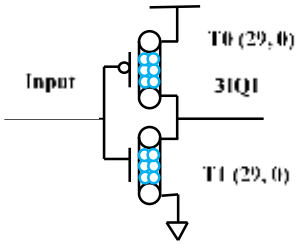

Fig.7(b) Proposed 3IQI

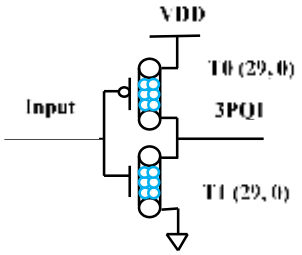

Fig .7(c) Proposed 3PQI

The modules which are used in Borrow Generation are 3NQI, 3IQI, 3PQI are shown in fig.7.

Compared to circuit of QHS using 4:1 MUX which is shown in figure 2 with 2:1 MUX which is shown in figure 5 it has reduced ten transistors. Table 4 shows the number of transistors for each circuit.

Table 4 Transistors Count

Circuits	No of Transistors
Proposed QHS using 4:1 MUX	88
Proposed QHS using 2:1 MUX	78

5. Simulation Results

The transient response of Quaternary half Subtractor (QHS) is show in Fig.8.

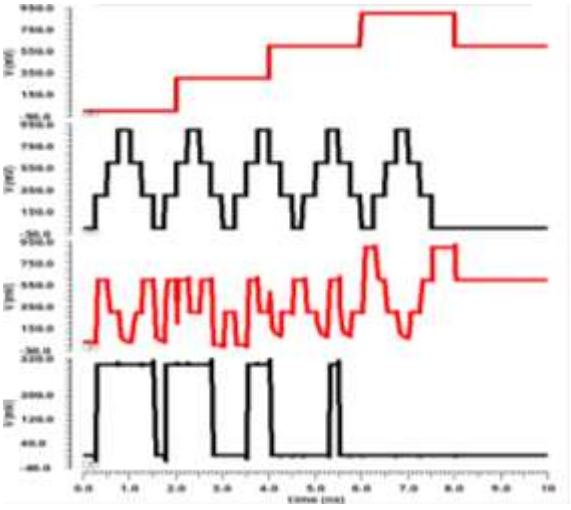

Fig.8 Transient response of Quaternary Half Subtractor

The performance of the proposed circuit is compared to that of the current circuit by varying the voltages from 0.7 V to 1.2 V, as shown in Table 5. The evaluation focuses on power consumption, delay, and the power-delay product (PDP). Although the proposed circuit exhibits lower power consumption, it incurs a greater delay than the existing circuit, resulting in an overall increase in the PDP.

6. Conclusion

Based on CNTFET, a novel Quaternary Half Subtractor is developed. In this design, ten transistors have been eliminated in comparison to the previous circuit by using a 2:1 multiplexer-based method. When compared to earlier Subtractor designs, the simulations of the proposed subtractor design demonstrate a improvement in power, energy and transistor usage.

Table 5 Power, Delay and PDP

Voltages(V)	Parameter	QHS using 4:1 MUX	QHS using 2:1 MUX
0.7	Power(nW)	12.93	9.102
	Delay(pS)	10.63	47.50
	PDP(aJ)	0.137	0.432
0.8	Power(nW)	23.07	18.79
	Delay(pS)	9.22	37.02
	PDP(aJ)	0.212	0.695
0.9	Power(nW)	175.9	113.6
	Delay(pS)	7.281	16.26
	PDP(aJ)	1.280	1.847
1.0	Power(nW)	968.6	843.4
	Delay(pS)	6.324	9.805
	PDP(aJ)	6.125	8.269
1.1	Power(nW)	3795.0	2782.0
	Delay(pS)	5.234	7.495
	PDP(aJ)	19.863	20.85
1.2	Power(nW)	5024.3	4926.2
	Delay(pS)	4.168	5.332
	PDP(aJ)	20.941	26.265

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

Sarada Musala conceptualized the designs and circuits.
P.Durga Vasavi carried out the simulation and the optimization.
Avireni Srinivasulu has Verified the results and validated the research outputs.
Cristian Ravariu has supervised and organized the research activity planning and execution, including mentorship external to the core team.

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Conflict of Interest
The authors have no conflicts of interest to declare that are relevant to the content of this article.