Design of High-Speed Low-power SRAM Cell using FinFET in the Stack Method for Medical Applications

MONIKA SHARMA, SANDEEP SINGH GILL, KANIKA SHARMA, BANOTH KRISHNA
Department of Electronics and Communication Engineering,
National Institute of Technical Teachers Training and Research-Chandigarh,
INDIA

Abstract: - This research presents a high-speed, low-power Static Random-Access Memory (SRAM) cell design utilizing the Stack Method, tailored specifically for medical applications. The Stack architecture using Fin-FET technology is employed to effectively reduce power consumption and access delays during both write and read operations. The proposed SRAM cell achieves notable power efficiency, with a power consumption of 35.9 nanowatts (nW). The delays are also significantly reduced with the write time of 168.377 picoseconds (ps) and read time of 212.35 ps. The circuit has been simulated in the Cadence Virtuoso EDA tool. This design can be used in medical applications because of its efficient performance parameters.

Key-Words: - CMOS, FinFET, Low-Power, High-Speed, Medical, SRAM, Stack method.

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1 Introduction

Static Random Access Memory plays an especially important role in modern technology to store data. One of the essential requirements of the SRAM in today's modern world is high speed and low power consumption. Figure 1 shows the circuit diagram of conventional 6T SRAM. The research tries to design the SRAM using a stack method which has better performance in terms of speed and power and can be incorporated into medical applications. The following explanation will explore the stack method regarding its method, goal, and result to establish its better performance.

Medical applications require devices that are reliable, fast, and power-efficient. Reliability is a major factor as human lives are at stake in case of malfunctionality of the equipment. Less power consumption is always desirable.

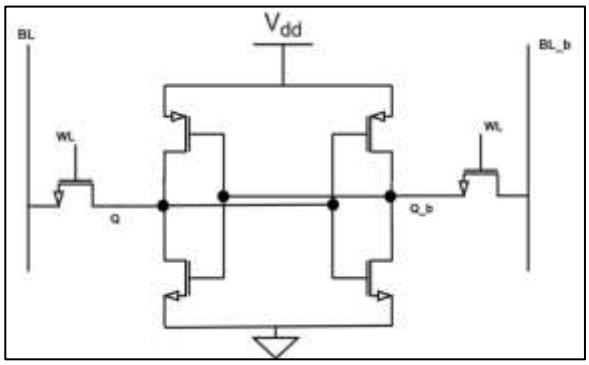

Fig. 1: Conventional 6T SRAM circuit diagram

Additionally, the ability of SRAM to operate in environments where reliability and accuracy are of paramount importance makes it suitable for use in medical equipment, where precision and the quick processing of large amounts of data play an important part in patient care and outcome.

2 Literature Review

The high-density 5T SRAM using a single bitline for read and write operation has been described to reduce power dissipation, [1]. While studying various SRAM configurations like 4T,5T,6T,7T,8T,9T, 10T,11T, it has been concluded that every configuration has certain trade-offs, [2]. Likewise in 7T SRAM, the write operation is performed by the single bitline to save power, [3].

6T SRAM and 8T SRAM have been studied and compared regarding their performance parameters, [4]. A new type of the 9T SRAM has been introduced with increased stability and lower power consumption, [5]. 10 T PPM based SRAM has been introduced which exhibits high stability and low leakage current, [6], along with it a Schmitt Trigger based 10 T SRAM has been proposed which has high SNM compared to 6T SRAM, [7].

Another ST based SRAM with better read and write operation and which can be used in the ultra-low power requirements was studied. It is also resistant to the process variation, [8].

In a bid to reduce power dissipation 10 T SRAM cell using power gated PMOS transistor was proposed, [9] and another 11 T SRAM which has good SNM and low power dissipation was studied, [10].

The numerical model for the simulation of SEE (single event effect) in realistic SOI FinFET was computed and have compared the nanoscale FinFET I-V characteristics, [11]. They have shown the importance of the correct physics model for accurate characteristics of FinFET.

The process variation effect on FinFET devices was also analyzed and was reported that power dissipation, WNM, RNM, and SNM of FinFET vary with the width of the load, driver, and access [12]. The FinFET with smaller widths have more deviations than the larger ones. As the temperature increases the SNM, and RNM decreases but WNM increases.

A new type of DG-FinFET SRAM with modification of the source potential of the NMOS transistor is designed which is more tolerant to the SEU, [13]. It has better performance compared to the standard DICE, but the area size is larger.

A comparison of the soft error study of the four different versions of double-gated FinFET with simultaneous and independent driven gates was done and it was concluded that the common double gate requires the highest amount of LET (Light Energy Transfer) to flip compared to independent DG-FinFET (Double Gated FinFET), [14]. Amongst the IG-FinFET (Independent Gate-FinFET), transistors in place of access device do not cause much degradation of SEU performance as compared to the transistors in the place of the inverters.

The 10 different topologies for the SEU hardness of the SRAM were compared and it was found out that the Flexible Pass Gate and Pass gate-opposite storage node amongst the IG-FinFET are the best options, [15].

Low power consumption IG FinFET is preferred over the SG (shorted Gate) but the PDP of the IG is more than that of the SG, [16]. Transistor sizing is an important parameter.

The fine grain and coarse-grain gating techniques were used to reduce power dissipation, enhancing SNM, [17]. A significant improvement in the gate control of the FinFET has been observed while using high-K dielectric material like (HFO2) i.e., Hafnium Oxide, [18]. The leakage current is reduced and hence reduces the short channel effect in the case of high-K dielectric material.

TID is impacted by the frequency of the radiation falling on FinFET, [19]. The circuit level parameters degrade i.e., gate delays become more, and the leakage current increases.

It has been analysed that the higher the Vth of the transistors, the more resistant they are to the radiation onslaught, [20]. In order to make SRAM more resistant to the atmospheric radiation, a new RHMD 10 T SRAM cell has been proposed which also has less power consumption, [21].

6T SRAM has been compared at the different technology nodes in terms of power, delay and SNM, [22] and in another study, 6T SRAM and 8T SRAM has been compared with regard to various performance parameters at 45 nm technology, [23].

Sleep transistor helps in reduction of static power as is studied, [24]. A novel approach to designing low-power SRAM cells with improved write ability has been proposed, [25]. The proposed design is based on stacked inverters and uses power gating, different supply voltages for different modes of operation, and other techniques to lessen power dissipation in static mode. The paper proposes that the design can be used in a less noisy environment where the voltage fluctuation is minimal.

The SRAM using a dual control stacked inverter has been designed and the proposed design has resulted in lower power consumption by 43.42% and reduces the delay by 77.05% when compared to the sleepy stack approach, sleepy keeper approach, and dual stack power gating, [26].

A double-ended low power SRAM which uses slow power stacked inverters was proposed leading in significant power reduction, [27]. By providing a low power supply during the read operation, power can be further reduced.

It has been analysed that the off-current, DIBL, on-current, and sub-threshold swing are highly dependent on process parameters like thickness and height of the fin, and oxide-thickness, [28].

It has been observed that the shape of the fin in FinFET transistors also plays an important role in the analysis of the short-channel effects like sub-threshold current, leakage current, etc., [29]. They have compared the short channel effects in the case of rectangular and trapezoidal-shaped fins.

A new 8T SRAM cell has been proposed and compared with the 6T and 8T SRAM which has better SNM and low power dissipation, [30]. Emphasizing on the importance of the Low power another 8T SRAM with restoration of the swing node is proposed, [31].

A reconfigurable SRAM which can be used as a sense amplifier to read data as well as in-memory computing was proposed, [32].

The new material transistor i.e. Carbon Nano tube FET which has better stability, low power dissipation and better performance when compared to the conventional MOSFET was proposed, [33].
The stacking method has been applied to reduce the leakage power, [34]. To reduce the power consumption by using transistors in stack was proposed, [35]. The write and read circuitry has been modified along with the use of the stack inverters to reduce leakage power, [36].

3 Methodologies

3.1 Analysis of Various SRAM Configurations using CMOS Transistors

6T SRAM, 8T SRAM, and 10T SRAM have been designed and simulated in Cadence Virtuosos in 45nm technology and the performance parameters (delay, power consumption, and static noise margin) are calculated.

3.2 Analysis of Various SRAM Configurations using FinFET Transistors

The performance parameters of 6T, 8T, and 10T SRAM are computed in Cadence Virtuosos while using FinFET transistors.

3.3 Stack Architecture-based SRAM Comparison with Another Configuration

The stack architecture-based circuit is compared with conventional SRAM, Forced-based SRAM and Forced NMOS based SRAM in Cadence Virtuoso in both CMOS and FinFET technologies.

Performance parameters:

a. **Stack Inverter Design:** The stack inverter design was compared with the CMOS inverter design. The performance parameters such as read delay, write delay, SMN, and power consumption were computed, compared, and analysed.
b. **Circuit Design of SRAM:** The SRAM was designed with the stack inverter using Cadence and its delay, power, and static noise margin were computed and compared with other SRAM configurations.

Sensitivity & error analysis: Sensitivity analysis is used to analyse the circuit under varying conditions of transistor size, voltage supply, temperature, noise margin, etc. It forecasts the reliability of the circuit.

Error analysis on the other hand takes into consideration the potential errors that could occur in the circuit during the read or write operation so that some error-correcting codes, or some redundant circuitry can be added to compensate for the error. The soft error is another major concern for SRAM cells exposed to the radiation which can be mitigated by introducing radiation-hardened cells.

3.4 Power Analysis

Power consumption is one of the deciding parameters while designing SRAM. A circuit with low power consumption is always desirable.

3.5 Timing Analysis

Timing analysis includes delay calculation during the read operation of the SRAM cell and delay calculation when some data is written into the cell. The smaller the value of the delay, the faster is the SRAM.

3.6 Static Noise Margin Analysis

SNM is the least amount of voltage required to alter the state of the cell. The higher the value of the SNM, the better is the reliability of the cell.

3.7 Comparative Analysis

A comparison between the designed stack inverter and various other SRAM configurations, based on the performance parameters was made and accordingly, the conclusion was established.

3.8 Validation and Optimization

We tried to adjust the circuit parameters to optimize the SRAM cell circuit by doing iterative simulation in the Cadence tool.

3.9 Robustness and Reliability Testing

To perform the robustness, and reliability test, the SRAM was simulated in various conditions like varying transistor sizing, etc.

The above-outlined methodology was used to design and evaluate the stack inverter-based SRAM design.

4 Result Analysis

The result obtained by analyzing the performance parameters of the SRAM circuit like power, delay

and SNM gives a favorable advantage to stack method design over other SRAM configurations.

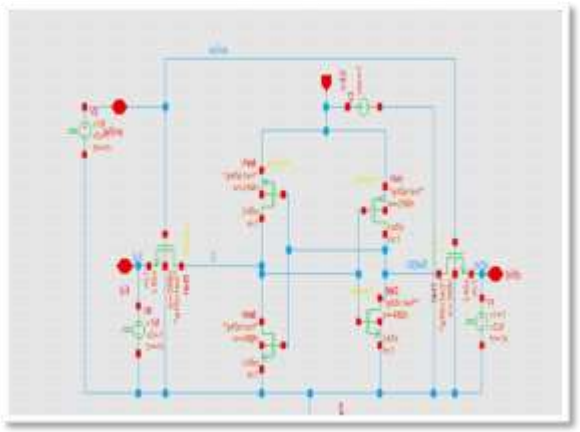

Fig. 2: 6T SRAM Circuit Diagram

a. CMOS Architecture Analysis: As shown in Figure 2 which represents the circuit diagram of 6T SRAM is implemented first using the CMOS transistor and then using the FinFET transistor with the help of the Cadence Virtuoso tool. In the 6T SRAM Circuit, the circuit is simple. As there is no separate read and write circuit its power consumption is more and is less stable.

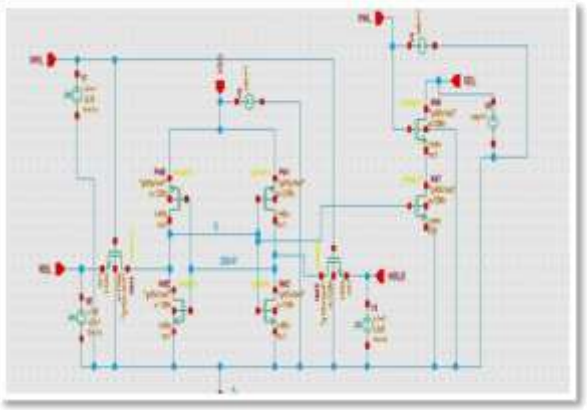

Fig. 3: 8T SRAM Circuit Diagram

Figure 3 is the schematic diagram of 8T SRAM implemented first using the CMOS transistor and then using the FinFET transistor using the Cadence Virtuoso tool. The read and write operations are isolated because of which 8T SRAM is more stable but consumes more area.

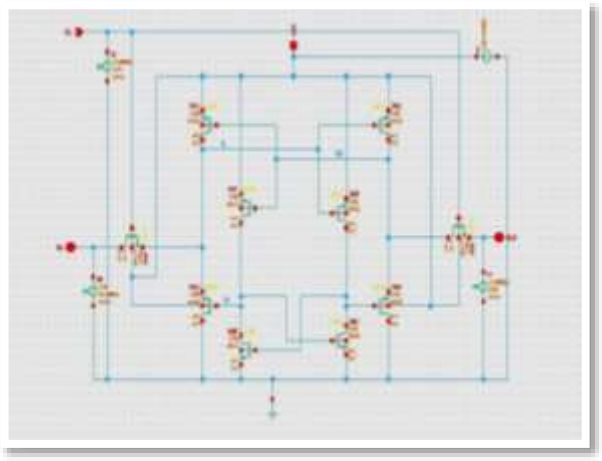

Fig. 4: 10T SRAM Circuit Diagram

Figure 4 is the schematic diagram of 10T SRAM implemented first using the CMOS transistor and then using the FinFET transistor using the Cadence Virtuoso tool. It is PP10T consisting of 10 transistors which includes 2 NMOS and 8 PMOS.

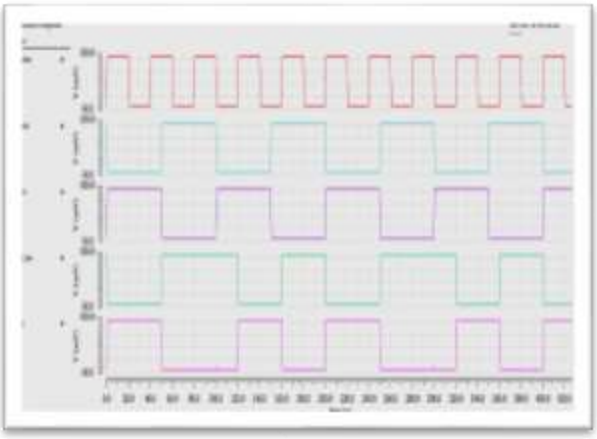

Fig. 5: Delay Propagation waveform

As shown in Figure 5 the delay waveform from which the propagation delay is calculated. Read Delay is calculated by first asserting the word line and then asserting both bit lines. Depending on the bit stored in the SRAM, there is a transition in either of the bit lines. This transition indicates if the stored bit is “0” or “1”. Write Delay is calculated when the word line is asserted and to write “1”, one of the bit lines is made high and the other bit line is made “0”.

Static Noise Margin which determines the sensitivity of noise towards the circuit has been computed. It can be observed that the SNM of Stack inverter-based SRAM is better as compared to the other configurations. When the sizing of the

transistors was not selected properly, we got the distorted butterfly curve indicating that SRAM has a low static Noise Margin and is not very reliable shown in Figure 6.

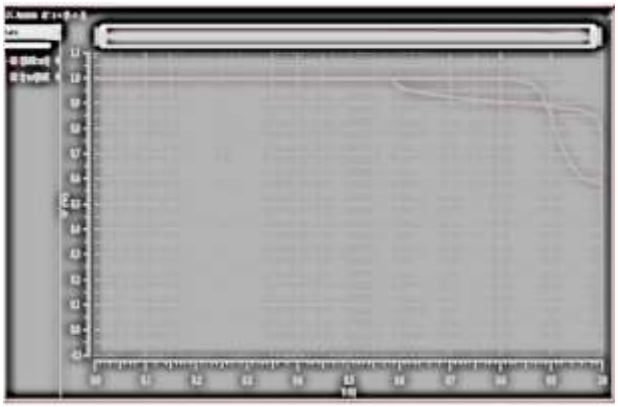

Fig. 6: Errored butterfly response

When the Sizing of the transistors was selected properly, a good butterfly curve was obtained, and the circuit has a good noise margin as shown below in the circuit.

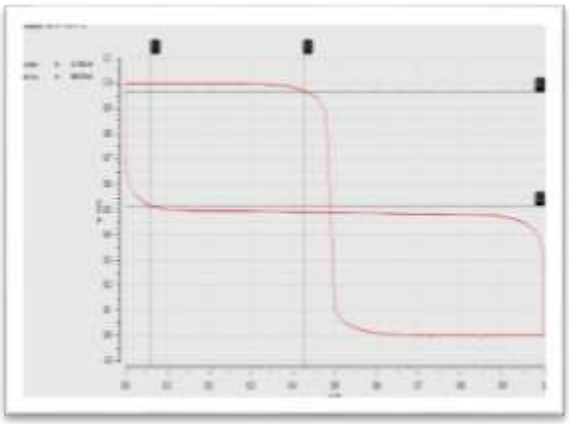

Fig. 7: Butterfly curve corrected response

The butterfly curve as shown above in Figure 7 is used to calculate the static noise margin. The butterfly curve is obtained by superimposing the voltage transfer char. of one inverter with that of the voltage transfer curve of the second inverter. SNM is calculated by the side of the largest square that can fit in the loops of the butterfly curve.

The above architectures of the 6T, 8T, and 10T SRAM have been analyzed in both CMOS and FinFET technologies and the following results are obtained. As can be observed from Table 1, 8T shows a considerable improvement in the power dissipation and the static noise margin as compared to 6T SRAM.

Table 1. 6T, 8T,10T CMOS Parameter Comparison

SRAM	Parameters	CMOS (45nm)
6T	Write Delay	286.833ps
	Power Dissipation	94.0908nW
	SNM	301.71mv
8T	Write Delay	424.479ps
	Power Dissipation	35.607ps
	SNM	376mv
10T	Write Delay	89.0277ps
	Power Dissipation	5.6136uW

b. **SRAM Cell Architecture Analysis in FinFET technology:** The architectures of the 6T, 8T, and 10T SRAM are implemented using FinFET transistors. The following results are obtained and as can be observed from Table 2 8T shows a considerable improvement in the power-dissipation and propagation delay when compared to the respective performance parameters in CMOS.

Table 2. 6T, 8T,10T FinFET Performance Parameter Comparison

SRAM	Parameters	FinFET
6T	Write Delay	242.448ps
	Power Dissipation	46.3959nW
	SNM	320.62mv
8T	Write Delay	237.025ps
	Power Dissipation	1.73482nW
	SNM	250mv
10 T	Write Delay	140.87ps
	Power Dissipation	11.131µw
	SNM	124.8555mv

As shown in Figure 8, Figure 9 and Figure 10 the respective performance parameters namely propagation delay, power dissipation and Static Noise Margin (SNM) of each of the 6T SRAM, 8T SRAM, and 10T SRAM have been analysed and the comparison is represented through the graph.

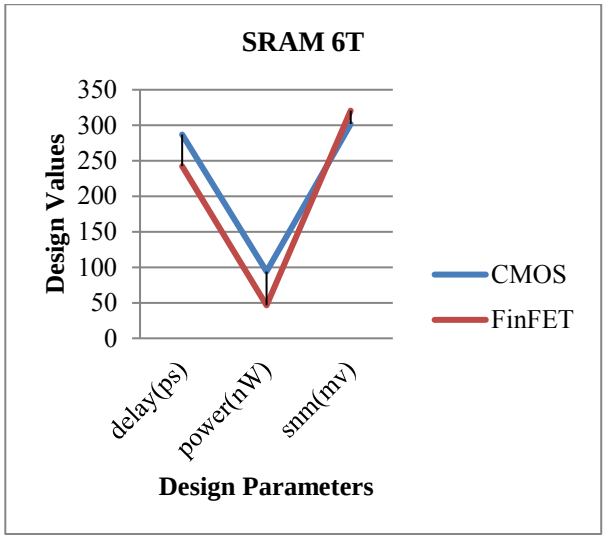

Fig. 8: Output Parameters Analysis of 6T SRAM

Figure 8 compares the CMOS and FinFET performance parameters namely propagation delay, power dissipation, and Static Noise Margin (SNM) of 6T SRAM in CMOS and FinFET technology. FinFET SRAM performs better than the CMOS SRAM as it has lower propagation delay, Less Power dissipation, and more SNM.

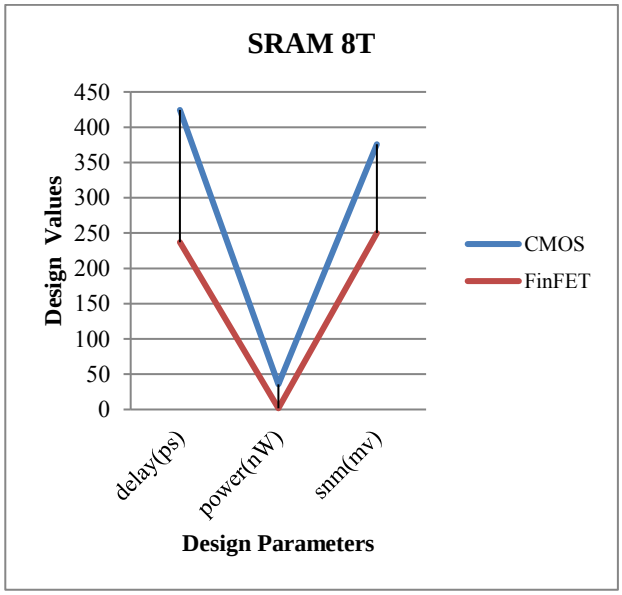

Fig. 9: Output Parameters Analysis of 8T SRAM

Figure 9 compares the CMOS and FinFET performance parameters namely propagation delay, power dissipation, and Static Noise Margin (SNM) of 8T SRAM in CMOS and FinFET technology. FinFET SRAM performs better than the CMOS SRAM with lower propagation delay and lower power dissipation.

Figure 10 compares the CMOS and FinFET performance parameters, namely propagation delay, power dissipation, and Static Noise Margin (SNM) of 10T SRAM.

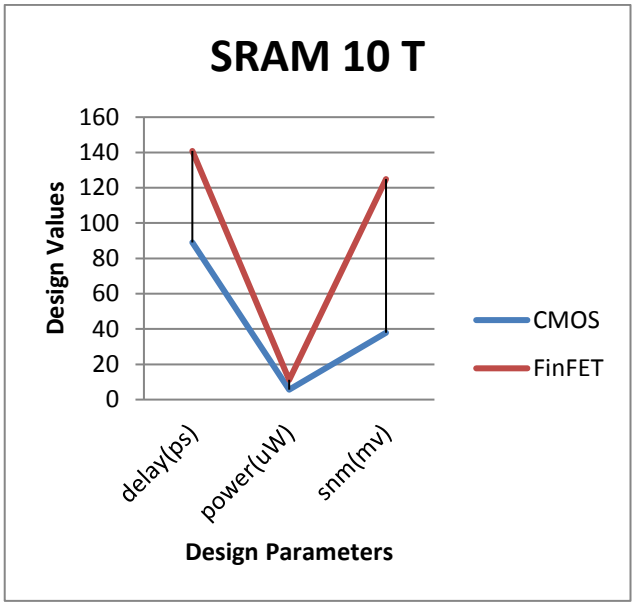

Fig. 10: Output Parameters Analysis of 10T SRAM

c. **STACK Architecture SRAM Analysis using CMOS and FinFET:** In logic gates, every NMOS and PMOS transistor gets split into two transistors. For NMOS, this division is beneficial for minimizing leakage current. The upper NMOS transistor encounters a rise in the source-to-substrate voltage, while the lower NMOS transistor undergoes an increase in the drain-to-substrate voltage. Both alterations aid in reducing the power lost in logic circuits. It is realized through the Cadence Virtuoso tool to calculate the performance parameters like power consumption, delay, and static noise margin. Stack architecture SRAM as shown in Figure 11 is analyzed in terms of performance parameters like delay time, power dissipation, and static noise margin. The results which are obtained after comparing the performance parameters of Stack architecture SRAM with Forced NMOS architecture and Forced PMOS architecture SRAM, are in favor of the designed SRAM.

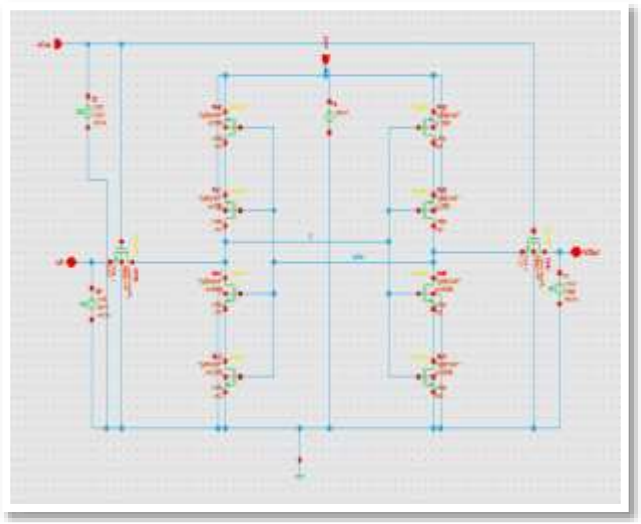

Fig. 11: Stack architecture SRAM

d. **Forced NMOS architecture SRAM:** Another method to minimize leakage power is the stack approach. It works by splitting a single transistor into two smaller transistors to benefit from a stacking effect. This method relies on the concept that a PMOS and NMOS device can be substituted by two equivalent NMOS and PMOS devices with half the width-to-length ratio (W/L). This technique resembles traditional CMOS, but it involves an additional NMOS at the bottom. By having two NMOS devices as shown in Figure 12, it leads to increased delay, resulting in reduced leakage power in the circuit.

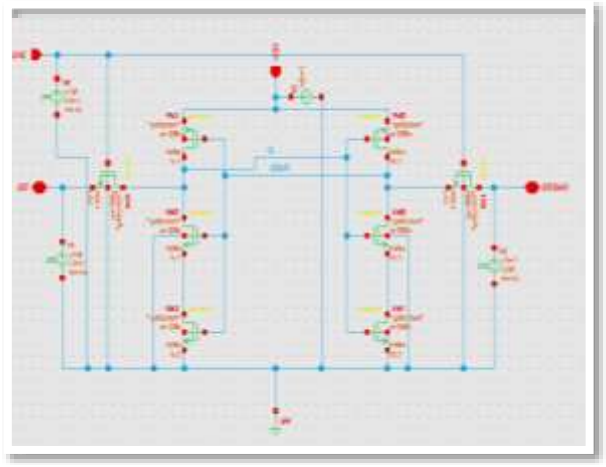

Fig. 12: Forced NMOS architecture SRAM

e. **Forced PMOS architecture SRAM:** This approach is the same as conventional CMOS but with an added PMOS in the upper part of the circuit as shown in Figure 13. A forced PMOS inverter is a type of logic gate that uses a PMOS (P-type Metal-Oxide-Semiconductor) transistor as the driving element.

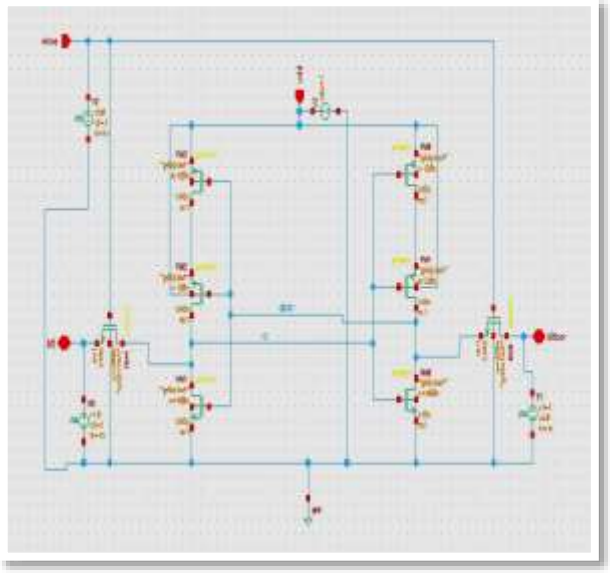

Fig. 13: Forced PMOS architecture SRAM

Table 3. Comparison between various SRAM Configurations

	Performance Parameters	CMOS	Fin FET
Stack transistor logic SRAM	Write Delay(ps)	242.396	168.377
	Read Delay (ps)	337.282	212.35
	Power (nW)	35.3	35.9
	SNM (mv)	364	364.33
Conventional 6T SRAM	Write Delay(ps)	286.833	242.448
	Read Delay(ps)	434.324	334.063
	Power (nW)	94.0908	46.3959
	SNM (mv)	301.71	320.62
Forced NMOS transistor SRAM	Write Delay(ps)	251.22	187.151
	Read Delay (ps)	269.439	214.632
	Power(nW)	70.090	42.1837
	SNM (mv)	350.07	363.76
Forced PMOS transistor SRAM	Write Delay (ps)	226.514	172.90
	Read Delay (ps)	434.867	339.62
	Power (nW)	40.4688	32,1024
	SNM (mv)	354	376.48

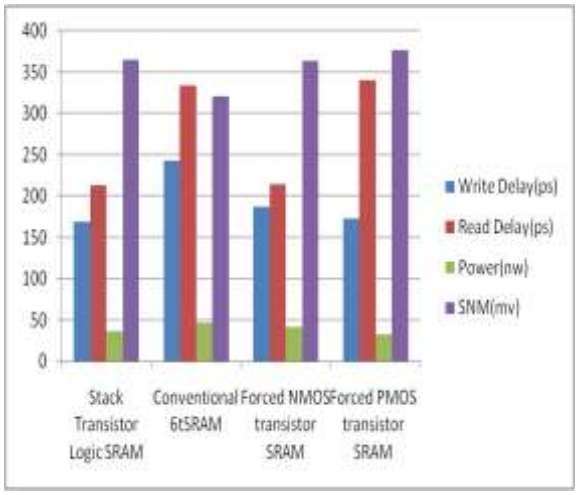

Fig. 14: Bar chart showing the comparison between different SRAM configurations

The comparison Table 3 is implemented in the Bar Chart for the visual representation. It is evident from Figure 14 that the Stack Transistor SRAM has a competitive edge over the other SRAM configurations in all the performance Parameters. It has lesser access time, lower power consumption, and high SNM which makes them suitable for devices where low power and high speed are required.

5 Conclusion

The research presents a favorable approach to SRAM cell design using the Stack Method, focusing on achieving a balance between high-speed performance and low power consumption for medical applications. The integration of the Stack Method has proven effective in enhancing power efficiency and minimizing access times, making the designed SRAM cell a viable solution for medical memory requirements. The achieved power efficiency of 35.3 nanowatts (nW) showcases a substantial reduction in power consumption, aligning with the growing need for energy-efficient memory solutions in the medical domain. Furthermore, the significant improvements in access times, with a write time of 242.396 picoseconds (ps) and a read time of 337.282ps, establish the SRAM cell as a high-speed memory option, crucial for real-time data processing and quick access to stored information. The high noise margin of 364mv further underscores the cell's resilience against noise-induced disturbances, ensuring consistent and error-free performance in challenging medical environments. Comparative analysis against conventional SRAM designs affirms the competitive advantage of the Stack Method-integrated SRAM cell. The robustness and reliability testing further validate the stability and consistent performance of the SRAM cell across various operational conditions, substantiating its suitability for integration in diverse medical systems.

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