

# Cascade PI-Fuzzy Based Position Optimization of Nonal Switched UPQC with DG for Power Quality Enhancement in IEEE 14 Bus System

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**Abstract**— An Unified Power Quality Conditioner (UPQC), owning the composition of shunt and series Active Power Filter (APF), has become a standard accepted solution in the area of current and voltage harmonics mitigation of a power system network. This paper furnishes a novel approach of nonal switched UPQC topology, supported with Distributed Generation (DG), aiming at the power quality enhancement and position optimization, placed at different locations in a standard IEEE 14 bus system. In addition to this, behaviour of the proposed topology is analysed using novel Cascade Proportional Integral (PI) - Fuzzy and Space Vector Pulse Width Modulation (SVPWM) as control algorithms and the outcomes are compared with the historical twelve switch UPQC topology. Simulation results of the proposal modelled in MATLAB/SIMULINK reveals the superiority of nonal switched UPQC and the optimal position of the proposed conditioner, for mitigating the harmonic issues in the standard IEEE 14 bus system.

**Keywords**— Nonal switched UPQC, IEEE 14 bus system, Cascade PI-Fuzzy, SVPWM, Power Quality (PQ).

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## 1. Introduction

In the current booming world, survival is inconceivable without the usage of electric power. Hence electrical energy plays a leading role. Assisting this, it is essential to promote the uninterrupted sustainable quality of electrical power to the end user, as many customer loads mandates the continual distortion free supply. But, the usage of soft switching devices and the nonlinear loads in the power system causes heating, harmonics, flickers and many other disturbances which will impact the system's availability and reliability.

To dilute the power quality issues, power quality monitoring equipment and power quality conditioners should be lodged in the distribution side to curb the harmonics, voltage sags, voltage swell, etc.

Rahul Virmani presented a work on the "Performance Comparison of UPQC and Active Power Filters for a Non-Linear Load". This work transparently remarks the advantages of implementing the UPQC into the power system, when compared with an APF. The control algorithm is recommended to diminish the harmonics, but with the need of excessive memory consumption [1].

The research titled "A Low Cost High Performance UPQC for Current and Voltage Harmonics Compensations" carried out by Quoc-Nam from Korea, suggest the use of low cost, high performing UPQC devices in a power system. They further proposed that the insertion of a capacitor in succession to shunt APF, will considerably curtail the voltage across the DC link [2].

Mohammed Abdul Ahad Yahiya's work on "Performance Analysis of DVR, DSTATCOM and UPQC for Improving the Power Quality with Various Control Strategies" compares the voltage quality enhancement techniques implemented using DVR, D-STATCOM and UPQC, actuated with PI controller and FLC, but are computationally rigorous because of the

complex algorithm with inefficient memory management [3].

Vinod Khadkikar revealed a new comprehensive review on the divergent possible UPQC topologies for single and three phase networks, to enhance the power quality [4].

Supplementing these, few conventional solutions for power quality improvement were still debatable due to inefficient algorithms, over consumption of memory and less impact on harmonics. Addressing these, there are noticeable advancements attempted in the literatures [5]-[10].

In this proposed methodology, the nonal switched UPQC topology is implemented along with DG, implanted in different locations of an IEEE 14 bus system which are controlled with the Cascade PI-Fuzzy and SVPWM control algorithms. Supporting this, the results are contrasted with twelve switch UPQC topology with the same stated control strategies. The simulation results, proving its effectiveness in harmonics reduction at different optimal location are presented.

The organization of the proposed work is as follows. Section II evokes the control strategies implemented in this research for UPQC. The detailed UPQC Configurations are given in Section III. Section IV presents the IEEE 14 Bus system. Section V documents the simulation results, and the conclusion of this work is reported in the Section VI.

## 2. Control Strategy

The key idea of control strategy is to calculate and facilitate the injection of required quantity of the voltage and current signals to improvise the compensation effect in the system. To

		Rate of change of error						
		LP	MP	SP	ZE	SN	MN	LN
Error	LN	ZE	SP	MP	MP	LP	LP	LP
	MN	SN	ZE	SP	MP	MP	MP	LP
	SN	MN	SN	ZE	SP	SP	MP	LP
	ZE	MN	MN	SN	ZE	SP	MP	MP
	SP	LN	MN	SN	SN	ZE	SP	MP
	MP	LN	MN	MN	MN	SN	ZE	SP
	LP	LN	LN	LN	MN	MN	SN	ZE

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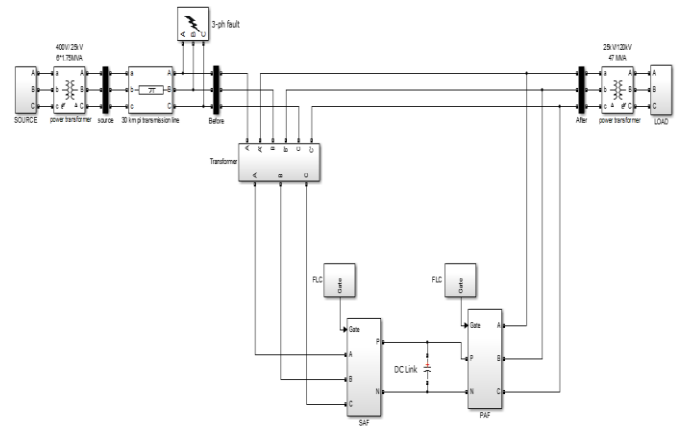


Fig. 6. Simulink model 3P3W UPQC configuration

The SAF and PAF are realized using IGBT bridge circuit with 12 switches. The 3- $\phi$  to ground fault having short circuit transition time of [0.15-0.3] s, is also simulated. Similarly, the other proposed configuration namely 9 switches topology is also modeled in the SIMULINK and successfully executed. The UPQC models are placed in between all the branches of an IEEE 14 Bus system. The UPQC are gated through cascade PI-Fuzzy and SVPWM separately and the harmonic analysis of voltage and current waveforms, (for phase A), measured before compensation and after compensation for both the two stated UPQC configurations are accomplished and the results are processed through the harmonic FFT analysis.

Fig. 7 shows the voltage waveforms before compensation and after compensation and Fig. 8 represent the current waveforms before compensation and after compensation for 3P3W configuration, placed between Bus 1 and Bus 2 of IEEE 14 Bus system. Both the figures indicating three phase waveforms in phases A, B and C are represented by the red, blue and green lines respectively.

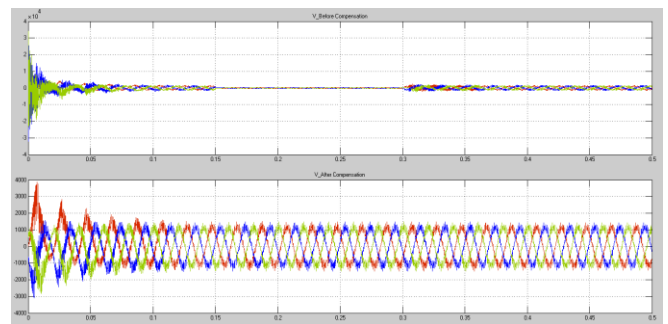


Fig. 7. Simulated results of voltage waveforms

To enable the comparative harmonic analysis of the two stated UPQC configurations, gated with two control strategies namely cascade PI-Fuzzy and SVPWM and to optimize their location, the proposed UPQC models are constructed in the MATLAB/SIMULINK environment. The Fig. 6 shows the detailed SIMULINK model of a 3P3W UPQC configuration, fired with cascade PI-Fuzzy method. It consists of a 3- $\phi$  voltage source rated 400V, 50Hz feeding a critical 3- $\phi$  load through the power transformers and transmission line.

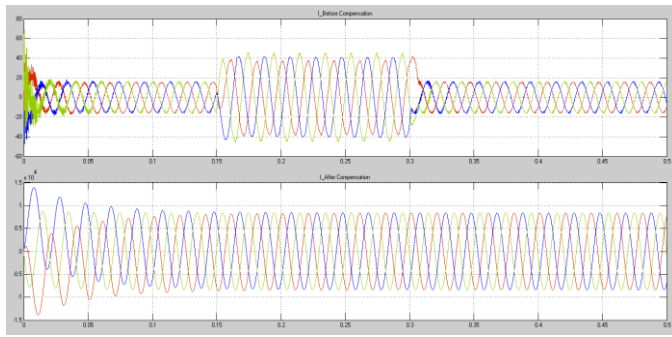


Fig. 8. Simulated results of current waveforms

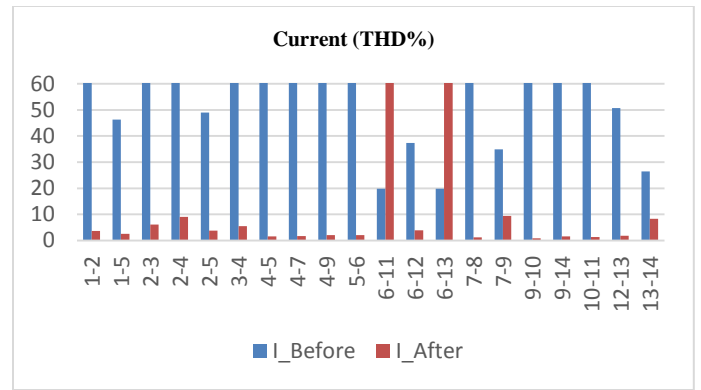


Fig. 10. Harmonic data of 3P3W topology with 12 switches and SVPWM

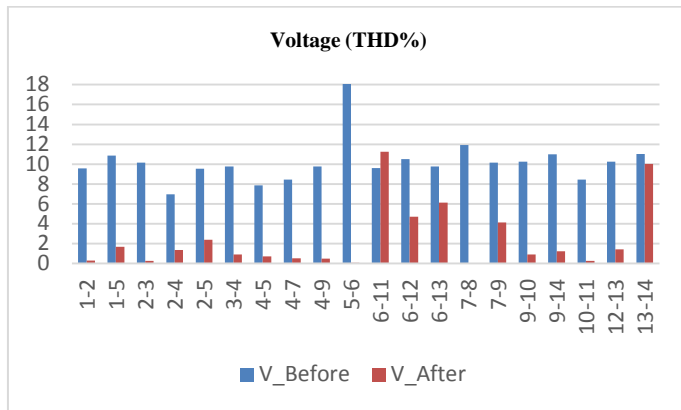


Fig. 9. Harmonic data of 3P3W topology with 12 switches and Cascade PI-Fuzzy

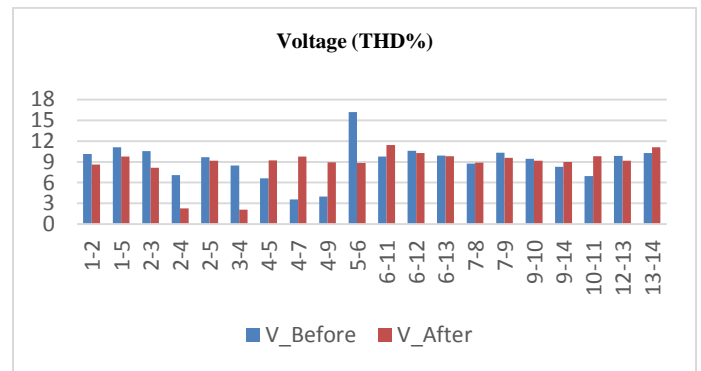
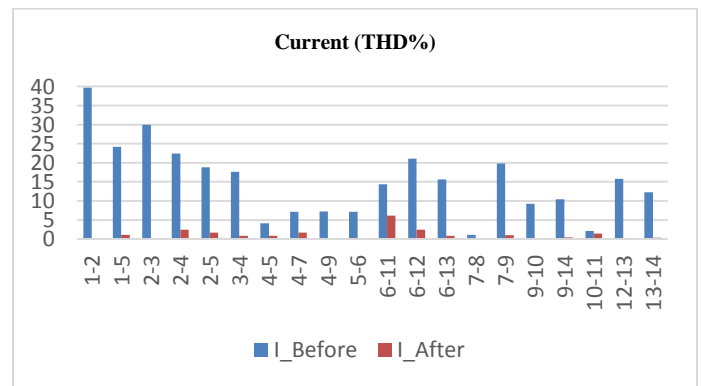
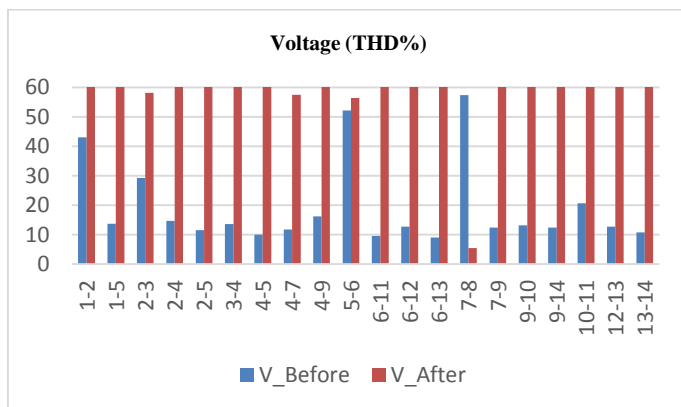


Fig. 11. Harmonic data of 3P3W topology with 9 switches and Cascade PI-Fuzzy



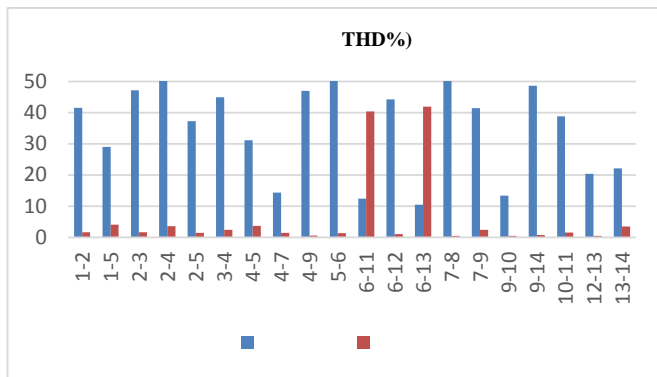


Fig. 12. Harmonic data of 3P3W topology with 9 switches and SVPWM

## 6. Conclusion

Power quality issues such as voltage sag and swell are most commonly occurred in the power distribution system. To overcome these issues, different topologies of UPQC are proposed in this paper. To enhance the power quality, 12 switch UPQC with Cascade PI-Fuzzy and 12 switch UPQC with space vector pulse width modulation, are implemented in MATLAB Simulink to minimize the voltage sag under different configurations. Further, the results of above stated configurations are compared with the novel 9 switch UPQC with cascade PI-Fuzzy and 9 switch UPQC with space vector pulse width modulation configurations, which are also simulated.

From the harmonic analysis, it is clearly indicated that the for 3P3W UPQC topology with 12 switches and gated with cascade PI-Fuzzy (Fig. 9), placing the UPQC in between bus 7 and bus 8 will be the optimal location, where both the voltage and current harmonic level can be drastically reduced to 0.03% and 0.07% respectively. If current harmonic is of concern, then the placing the UPQC in between bus 2 and bus 3 is an optimal choice, where the current harmonic level is reduced to 0.04%.

For 3P3W UPQC configuration with 12 switches and gated with SVPWM (Fig. 10), placing the UPQC in between bus 7 and bus 8 will be the optimal placement, where the voltage harmonic level can be managed to 5.43% and current harmonic level can be controlled to 1.16%. If current harmonic is of interest, then the placing the UPQC in between bus 9 and bus 10 is an optimal choice, where the current harmonic level is reduced to 0.85%.

Similarly, for 3P3W UPQC topology with 9 switches and gated with cascade PI-Fuzzy (Fig. 11), placing the UPQC in between bus 3 and bus 4 will be the optimized position of placement, where the voltage and current harmonic level can be quenched to 2.08% and 0.84% respectively. If current harmonic is of importance, then the placing the UPQC in between bus 7 and bus 8 is an optimal one, where the current harmonic level is reduced to 0.04%.

Likely, for 3P3W topology with 9 switches and gated with SVPWM (Fig. 12), placing the UPQC in between bus 5 and bus 6 will be the optimized target, where both the voltage and current harmonic level can be hindered to 5.32% and 1.37% respectively. If current harmonic is of concern, then the placing the UPQC in between bus 7 and bus 8 is an optimal choice, where the current harmonic level is reduced to 0.43%.

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## Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

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## Conflict of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article.

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