# Low Voltage Low Power And High Speed Opamp Design Using High-K Finfet Device

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Abstract— In this paper, operational amplifier circuit is designed using model parameters of high-k FinFET in 22nm technology. The conventional design expressions for MOSFET based OPAMP design are fine tuned to design FinFET based OPAMP. The OPAMP design is suitable for use as sub circuit in ADC design as it supports low voltage, high speed and low power dissipation. The transistor geometries are identified so as to achieve high performance and energy efficient OPAMP. Schematic capture is carried out using Cadence tool. From the simulation studies, the designed OPAMP has a unity gain bandwidth of 100 GHz and slew rate is equal to 1V/μS. The maximum power dissipation of differential amplifier circuit is 800nW and hence suitable for all low power analog and digital circuits.

Keywords--- FINFET, DIFFERANTIAL AMPLIFIER, OPAMP, HIGH-K, DG-FET

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## 1. Introduction

Role of high performance Analog to Digital Converters (ADC) is indispensable in signal processing applications as they provide interface between the sensor that acquire the signal from real world to the digital signal processor that processes the real world signal in digital domain. Successive Approximation Register (SAR) ADCs due to their advantages in terms of power dissipation and with 50% of the circuit topology being digital are widely used in most of the signal processing applications. SAR logic requires more steps to find the equivalent digital pattern for every analog input and hence requires longer time period compared with flash ADC that completes the operation faster. Design of asynchronous ADC is presented by Hsieh et al. [1] to remove the clock from the SAR logic to reduce conversion time, however the conversion time is observed to be still not improved with use of multiple comparators with reset operation in every step. High resolution ADCs operation at 150 MSPS and low power dissipation have been presented in [2], [3]. Time-interleaved ADCs or pipelined ADCs demonstrating both high speed operation and high resolution is presented in [4] based on SAR logic. Tai-Ji An et al. [5] in their work have designed asynchronous pipelined SAR ADC in 28nm CMOS technology demonstrating power dissipation of less than 3.5 mW operating at 160 MSPS. With two stage pipeline operation, power dissipation and die area are the major limitations. It is observed that the SAR based ADC is suitable for high resolution but suffers from lower speed due to the presence of SAR logic. Many schemes have been presented in literature for design of SAR ADCs to achieve high resolution, low power and faster conversion time. Circuit topologies and scaling of MOS transistors are two prominent methods reported in literature. Scaling in MOS transistor sizing and power supply has demonstrated improvement in ADC efficiency [6]. It is observed that lower power supply diminishes Signal to Noise Ratio (SNR) in analog circuits [7]. CMOS technologies operating in subthreshold regions are used in ADC design to optimize energy efficiency with trade-off between speed, noise performance and area requirement [8]. Energy efficiency of CMOS technology limits the energy efficiency in CMOS based ADCs particularly in low resolution ADCs. Leakage current and lower yield due to device to device variation are major challenges in sub-22nm CMOS technology. It is required to look for an alternative devices other than MOS transistors to achieve energy reduction [9]. Double Gate FETs (DG-FET) or Multi Gate FET (MG-FET) is one such device that has been identified to overcome these challenges. MG-FET is emerged has one of the promising device for low voltage applications development because of its energy efficiency due to sub-thermal switching characteristics. In MG-FET the channel width is very small and there are more than two gate contacts or in particular in DGFET there are two contacts on both sides of the channel to effectively control the flow of current in the channel. MGFET has not only the advantage of minimizing short channel effects, and also has the better control of the active channel by the gate electrode, but also of being compatible with the conventional planar CMOS technology. Vahid Baghi Rahin and Amir Baghi Rahin [10] in their work have presented low voltage and low power OPAMP using FINFETs that is designed to achieve DC gain of 52 dB with UGB of 6.4 MHz, power dissipation of less than 58 microW and phase margin of 71 degrees using 32nm device models. The phase margin of 71 degrees ensures very stable OPAMP design but affects the steady state response. For high speed ADC circuits, it is required to design OPAMP that can operate in few GHz range and still consume very less power dissipation. This is achieved by adopting suitable design procedure in identifying transistor geometries. Systematic approach is required to be followed to carry out design of transistor geometries. In this paper, FinFET based OPAMP design is carried out that could be used for design of high resolution, high speed, low power ADC based on SAR logic in 22nm technology.

## 2. FinFET

FinFET is similar to MOSFET structure and has advantages such as high drain current, low switching voltage and very less leakage current. FinFET was first developed in University of California by professors Chenming HU, Tsu-Jae King-Liu and Jeffrey Bokor [11]. In DG-FET the transistor efficiency is increased as there are two gates controlling the flow of current and the size of the channel is reduced hence gate to channel coupling is doubled and short channel effects are minimized. DG-FET current drive capability is doubled as compared with MOSFET and hence the device can operate at low input voltages and also below threshold voltages resulting in very low power dissipation [12], [13]. FinFET device with two gates wrapped around the surface of a thin Si body is as shown in Figure 1.The voltage applied on the gate controls the flow of current in the channel between the source and drain. The structure of FinFET is similar to MOSFET with the only difference of two gates.

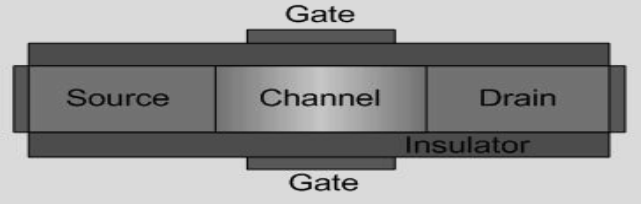


**Fig. 1 Structure of FinFET (Double gate) [13]**

The circuit topology or the small signal model of the FinFET is as shown in Figure 2. The intrinsic circuit comprises of parasitic capacitances $C_{gd}$, $C_{gs}$ and $C_{ds}$ along with the parasitic resistance $R_{gd}$, $R_{gs}$, $R_{ds}$ and $R_{sub}$. The capacitances $C_{pg}$ and $C_{pd}$ are considered at low frequencies with pinch-off condition. The parameters $L_g$, $R_g$, $R_s$ and $R_d$ are computed considering $V_{gs}$ above pinch-off.

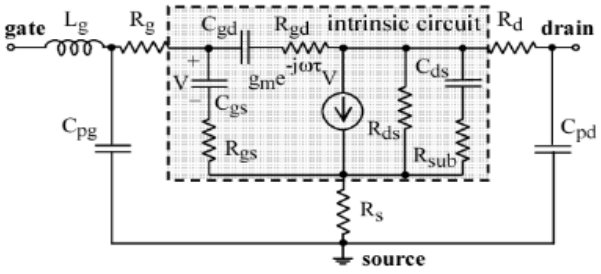


**Fig. 2 Small signal equivalent circuit for FinFET [15]**

The small signal model and model file of FinFET considered from Predictive Technology Model (PTM) is considered for design of ADC. The device parameters are presented in Table 1. The source doping and drain doping concentration based on Gaussian doping is considered at 1e+19/cm$^{-3}$, the dielectric constant of channel is 11.7 and the dielectric constant of insulator is 3.9. The bandgap and affinity of channel material is considered at 1.12 eV and 4.05 eV with gate contact work function of 4.6 eV. Mobility of electrons and saturation velocity is considered at 1400 cm$^2$/Vs and 1.07e+07 cm/s. The equivalent circuit model is having gate, source and drain terminals along with the intrinsic circuit. Considering these structural and electrical properties for FinFET the device model is simulated for its input and output characteristics.

**Table 1 FinFET device parameters**

| Parameter | Value (Proposed work) | Value [10] |
|---|---|---|
| Channel length | 22 nm | 32 nm |
| Oxide thickness 1 | 2.5 nm | 1.6 nm |
| Oxide thickness 2 | 2.5 nm | 1.6 nm |
| Gate length | 22 nm | – |
| Source/drain extension length | 50 nm | 32 nm |
| Gate to source/drain overlap | 2 nm | – |
| Work function | 4.6 eV | 4.5 eV |
| Source/Drain doping | $1\underline{x}10^{19}$ cm$^{-3}$ | $2\underline{x}10^{20}$ cm$^{-3}$ |

Figure 3 presents the input and output characteristics for the FinFET considered with the structural parameters as in Table 1. It is also known as the V-I Characteristics of FinFET.The parameters chosen in this work is compared with the parameters that have been considered in [10]. The technology selected in this work is 22 nm. The input is obtained by setting the drain voltage at 0.5 V and 1V. The output characteristic is obtained by setting the gate voltage between 0 Vto 1 V with incremental step so 0.1 V.

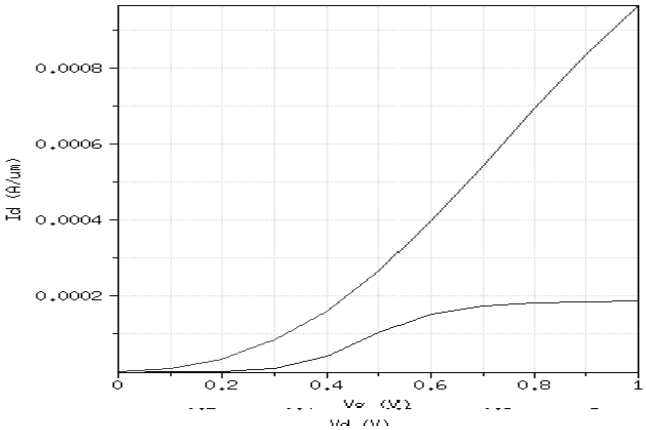


**Fig. 3 Characteristics of FinFET**

Figure 4(a) and 4(b) represents the V-I characteristics of FinFET considered at 22 nm technology with high-K dielectric. Figure 5 presents the variation in output characteristics of FinFET with different transistor widths.

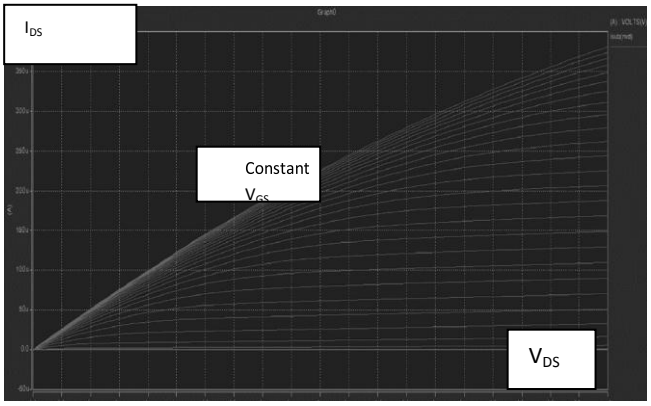


**Fig. 4(a) Output Characteristics Plot of $V_{DS}$ Versus $I_{DS}$ at Constant $V_{GS}$**

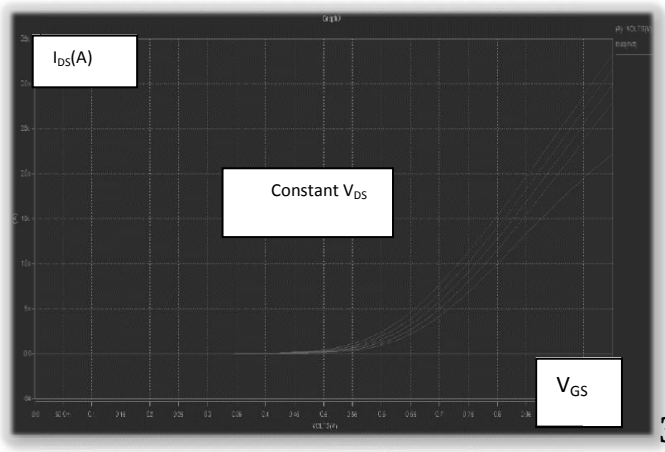


**Fig 4(b) Input Characteristics $V_{GS}$ Versus $I_{DS}$ at constant $V_{DS}$**

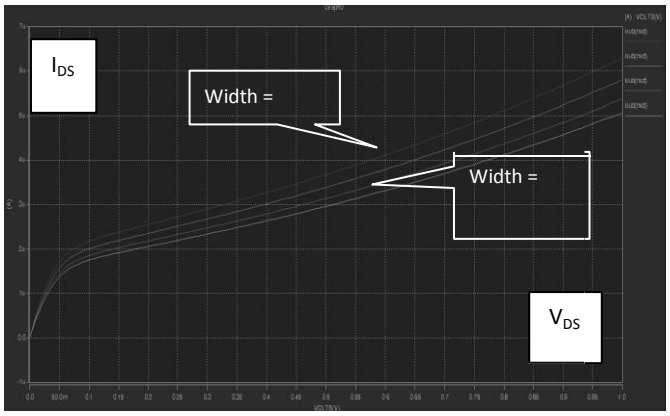


**Fig. 5 Output characteristics for varying width of High-k FinFET 22 nm technology**

Figure 6(a) presents the power dissipation and transfer characteristics of inverter based on FinFET device. The maximum power dissipation is observed to be less than 800nW and transition width is less than 0.12 V. Figure 6(b) presents the leakage current analysis for FinFET based inverter circuit. The leakage current during positive switching and negative switching current is observed to be less than 9µA.

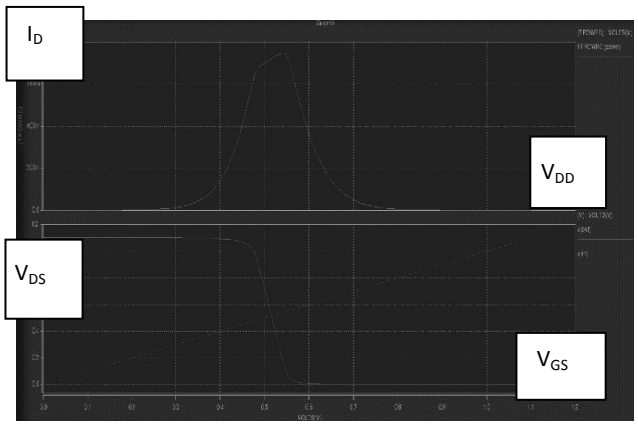


**Fig. 6(a) Power dissipation and transfer Characteristics of Inverter**

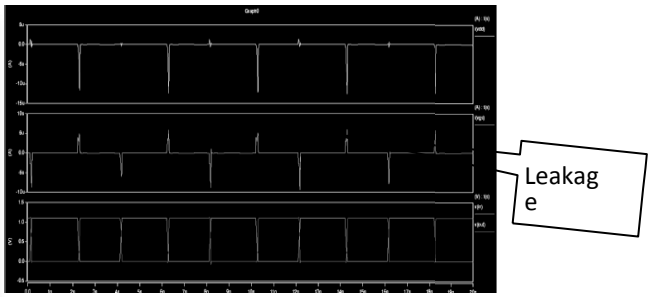


**Fig 6(b) Leakage Current analysis of Inverter characteristics for 22nm high-k FinFET**

# 3. Opamp Design

It is required to design OPAMP considering FinFET as the basic device.The characterization of FinFET model is presented in [14]. The threshold of FinFET is considered as 0.25V, subthreshold slope (SS) is 65mV/dec, $g_{ds}$ and $g_m$ at 0.3V of $V_{DS}$ and $V_{GS}$ is 8.97 µS/µm and 0.18 mS/µm, respectively. $g_m/I_{DS}$ at $I_{DS}$ = 10µA/µm is 27/V, on-current and off-current is 6.20 µA/µm and 3.3nA/µm, respectively. The maximum operating frequency of FinFET is 140 GHz with noise power of 1.15e-13 Hz-1 at $V_{GS}$ = 0.3V and 10GHz operating frequency. Considering these model parameters from the technology file and model file, the two-stage OPAMP is designed. Figure 7 presents the circuit schematic of two-stage OPAMP realized using FINFETs.

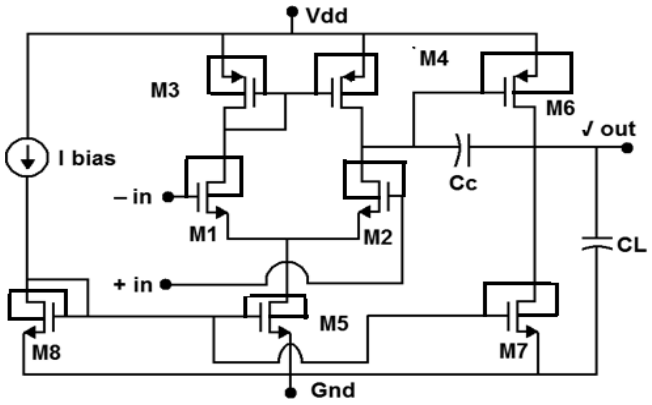


**Fig.7 FinFET based OPAMP [10]**

Table-2 presents the OPAMP design specifications considered for the requirement of SAR ADC design. The slew rate is assumed to be greater than 1V/ µS and the power dissipation is set to be less than 10 µW with mobility factors considered from model file the constants $K'_p$ and $K'_n$ are computed.

**Table-2 OPAMP design specifications**

| Parameters | Value |
|---|---|
| Slew Rate = SR | >1V/µS |
| $V_{out}$ range | = ±1.5V |
| ICMR | = 0.15 to 1.2V |
| Power Dissipation | ≤ 10µW |
| $V_{th} = \|V_{tp}\|$ | = 0.25V to 0.45V |
| $K'_p = \mu_p C_{ox}/2$ | = –455 µA/V² |
| $K'_n = \mu_n C_{ox}/2$ | = 1085 µA/V² |

Design procedure for MOSFET based OPAMP is discussed in detail by Allen Hollberg [15]. In this work the design procedure is fine tuned to compute the transistor geometries of FINFETs for OPAMP circuit schematic. Table 3 summarizes the design procedure for FinFET based OPAMP design.

**Table-3 Design procedure for OPAMP design**

| Requirement | Expression for MOSFET based OPAMP design | Tuning required for FinFET design |
|---|---|---|
| Meeting compensation capacitor from the load capacitor for a 60 phase shift | $I_5 = SR \cdot C_c$ | Similar to MOSFET |
| Finding of bias current from the slew rate and compensation capacitor | $I_5 \cong 10\left(\frac{V_{DD} + \lvert V_{SS}\rvert}{2 \cdot T_s}\right)$ | |
| Calculating M3 transistor sizing from the ICMRspecifications | $S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\max) - \lvert V_{T03}\rvert(\max) + V_{T1}(\min)]^2} \geq 1$ | Similar to MOSFET |
| Finding Transconductance of the $S_1$ transistor from the gain bandwidth specification | $\frac{g_{m3}}{2C_{gs3}} > 10GB.$ | Limits set to 140GB |
| Calculating $S_1$ transistor sizing from the Transconductance | $g_{m1} = GB \cdot C_c \Rightarrow S_2 = \frac{g_{m2}^2}{K'_2 I_5}$ | Use model file parameters for mobility |
| Calculating VDS of transistor $S_5$ from ICMR specification | $V_{DS5}(\text{sat}) = V_{in}(\min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\max) \geq 100\ \text{mV}$ <br> $S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$ | Set upper threshold to 10 mV and use mobility constant from model file |
| Finding transconductance of $S_6$ from $gm_1$ | $g_{m6} = 2.2g_{m2}(C_L/C_c)$ <br> $S_6 = S_3\left(\frac{g_{m6}}{g_{m3}}\right)$ | Similar to MOSFET |
| Calculating $S_6$ transistor sizing from the Transconductance of $gm_6$ and $gm_4$ | $I_6 = (S_6/S_4)I_4 = (S_6/S_4)(I_5/2)$ | Similar to MOSFET |
| Calculating $I_6$ | $I_6 = (gm_6)^2/2\ K'6(W/L)_6$ | Use model file parameters for mobility |
| Calculating of $S_7$ from the $S_5$, $I_6$ and $I_5$ | $(W/L)_7 = (W/L)_5 * I_6 / I_5$ | Similar to MOSFET |
| Finding $V_{min}(out)$ considering W7 | $V_{min}(out) = V_{DS7(sat)} = \sqrt{}(2.I_6/ K'(W/L)_7)$ | Use model file parameters for mobility |
| Calculating the power dissipation of OPAMP | $A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_5(\lambda_6 + \lambda_7)}$ | Lambda is approximately zero in FinFET (assumed to be very less number) |
| Verifying the gain of the two-stage operational amplifier | $P_{diss} = (I_5 + I_6)(V_{DD} + \lvert V_{SS}\rvert)$ | |

From [14] and from Figure 3 it is observed that with gate voltage change of 0.1 V the drain current increases by 200 µA demonstrating the high current handling capability of FinFET and hence identifying transistor geometries is an important factor for design of high performance OPAMP with high speed and low power requirement. Considering the expression in Eq. (1), the $g_m/I_{DS}$ of FinFET variation with respect to $V_{GS}$ for FinFET is expressed considering the steep slope (SS) which is required to overcome the limitations of CMOS which is of 40 $V^{-1}$. Increasing $g_m/I_{DS}$ can increase power dissipation in FinFET which can be controlled by reducing $V_{DD}$ for design of analog circuits. It is required to consider trade-off between $g_m/I_{DS}$ and $f_T$ ($=g_m/2(C_{gs}+ C_{gd})$) in CMOS based OPAMP design,

however with high $g_m/I_{DS}$ the desired $f_T$ (maximum requirement) can be simultaneously achieved in FinFET based OPAMP design. In FinFET based OPAMP design energy saving is achieved by lowering $V_{DD}$ without affecting maximum operating frequency, drive strength and wider operation bandwidth, making the OPAMP suitable building block for SAR based ADC design.

$$\frac{\partial I_{DS}}{\partial V_{GS}}\left[\frac{1}{I_{DS}}\right]=\frac{g_{m,\,FINFET}}{I_{DS}}=\frac{\partial \mathrm{In}I_{DS}}{\partial V_{GS}}=\frac{\mathrm{In}10}{SS} \qquad \ldots(1)$$

The above equation (1) describes about the ratio of transconductance($g_m$) and Drain to Source Current ($I_{DS}$) with respect to FinFET[14]. In FinFET effective mobility is higher due to non-doping of channels and hence higher $g_m$ is achieved, significantly reducing channel length modulation factor (λ). With the reduction in λ, the gain factor significantly increases in OPAMP design as indicated in Table 3, which is compensated by reducing the current flow in transistor M5 and M6 thus reducing the transistor width by half as compared with MOSFET transistor design. Based on the expressions and design procedures presented in this section the transistor geometries of OPAMP design are computed and is presented in Table-4.

**Table-4 Transistor geometry computed considering design procedure in Table 3**

| Transistor Number | W in nanometres for MOSFET based design | W in nanometres for FinFET based design |
|---|---|---|
| M1 | 200 | 100 |
| M2 | 200 | 100 |
| M3 | 1200 | 600 |
| M4 | 1200 | 600 |
| M5 | 800 | 400 |
| M6 | 1600 | 800 |
| M7 | 1400 | 700 |
| M8 | 800 | 400 |

# 4. Results & Discussion

The FinFET based OPAMP circuit design is carried out considering PTM 22nm high-K model with double gate configuration. The design is captured in Cadence environment and the SPICE code simulations are also carried out using HSPICE simulator. Device configuration and FinFET structure model is captured from FinFET simulator from online simulator from nanohub.org. PTM model files obtained are also configured in Electric tool for validation process device models. The schematic capture in Cadence environment is analyzed for DC and AC response. Output voltage swing, CMRR, PSSR and settling time are also analyzed. Frequency response of the designed OPAMP is also captured for different input voltages from which the gain margin and phase margin is computed. Figure 8 presents the gain margin and phase margin response for OPAMP. The design specifications were set to 60° of PM, from the simulation results the PM is obtained to be of 58°. The UGB measured from the response plot is found to be of 100 GHz demonstrating the wider operating range of the designed OPAMP. Figure 9 presents the step response of OPAMP with input and output response.

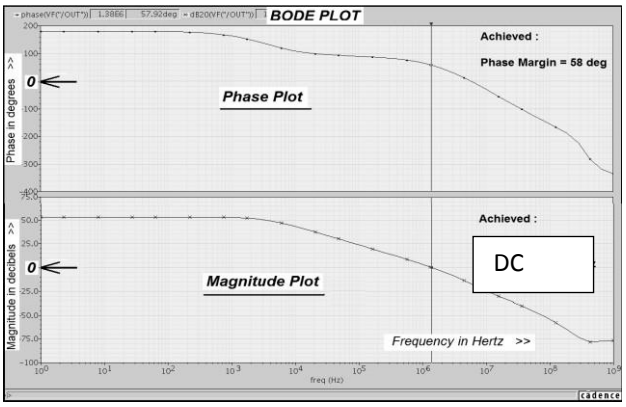


**Fig. 8 Frequency response representing gain and phase margin**

The input is set without any rise time delay and the output is observed to have rise-time of less than

1.2 ns and overshoot of less than 4%. With rise time and overshoot meeting the desired specifications the OPAMP design is suitable for high speed applications. Figure 10 presents the slew rate measurement of OPAMP by setting the load capacitance to 0.3pF. The slew rate is found to be 1V/μS. With high drive current in FinFET based OPAMP constituted by M5 transistor ensures that slew rate is greater in the OPAMP circuit demonstrating quicker response. The UGB is observed to be very high value of nearly 100 GHz and accordingly the $C_C$ capacitance is set to a very low value to meet high UGB requirements.

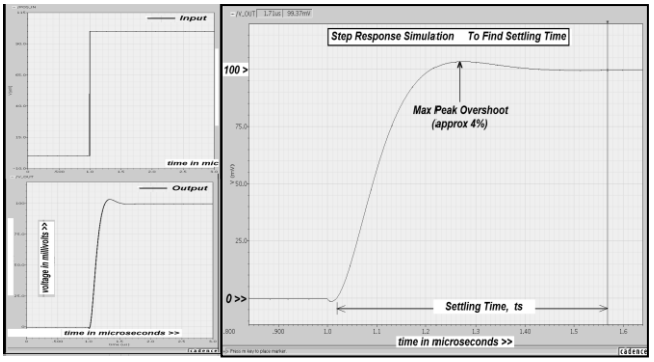


**Fig. 9 Step response representing overshoot**

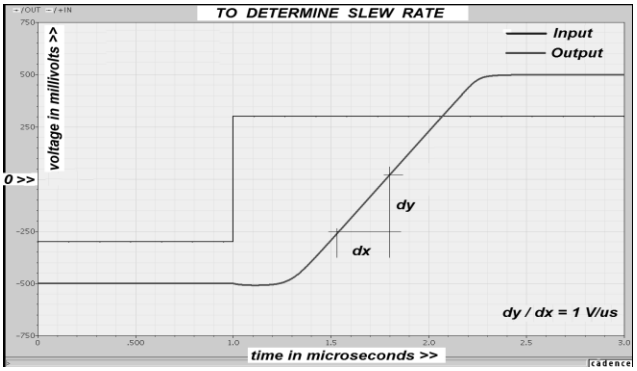


**Fig. 10 Computing slew rate of OPAMP**

The settling time of OPAMP required to be very short and is dependent on bandwidth and slew rate of the OPAMP. A trade-off is required to be arrived at and hence in this work the phase margin is appropriately set to 58 leading to stable and faster transition time.

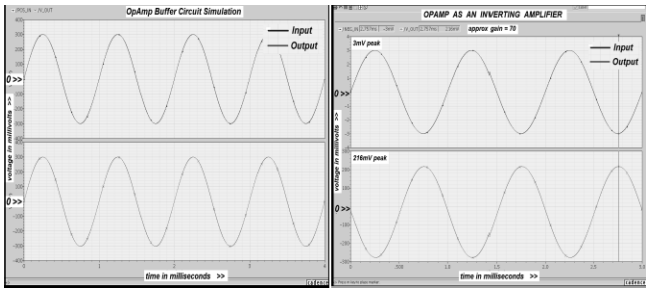


**Fig. 11 OPAMP response in noninverting and inverting configuration**

Figure 11 presents the inverting and non-inverting configurations of OPAMP and the results demonstrate the functionality of the circuit with the required gain factor of 70. Figure 12 presents the comparator design of OPAMP circuit with DC voltage set to 0V. The comparator output switches between +/– Voltage rails demonstrating functionality.

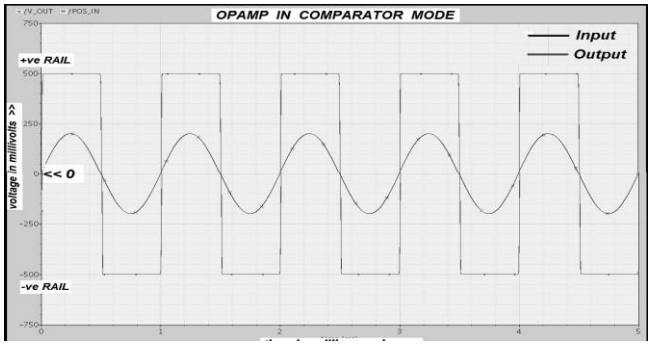


**Fig. 12 OPAMP configured as comparator**

The results obtained in this work for the OPAMP design is compared with the work carried out in [10]. The comparisons in terms of PSRR, UGB, SLEW RATE and power dissipation is presented in Table 5 that parameters are considered at operating at 10 GHz frequency.

**Table-5: Comparison of parameters in OPAMP Design**

| Parameters in OPAMP Design | Existing Literature using 32nm FinFET technology[10] | Present work using 22nm FinFET technology | Percentage Improvement |
|---|---|---|---|
| **DC Gain** | 42 dB | 53 dB | 20.75% |
| **PSRR** | 32.4dB | 45dB | 28% |
| **SLEW RATE** | 26.36mV/µS | 1V/µS | 97.36% |
| **Power Dissipation** | 58µW | 12µW | 79% |
| **FOM** | 5.3 | 52.5 | 89.9% |

Comparing the performances in terms of PSRR, slew rate, power dissipation and Figure of Merit (FOM), the proposed FinFET based OPAMP is superior in its performances. The systematic design approach has enabled to design the transistor geometries and selection of suitable device parameters. Improvement of DC gain by 20.75% is achieved along with PSRR by28%.Also there is an improvement of slew rate by 97.36% and Power dissipation by 79% is achieved.

# 5. Conclusions

In this work an Operational Amplifier Circuit is designed that could be used for design of high resolution, high speed, low power ADC based on SAR logic using model parameters of high-k FinFET in 22nm technology. The FinFET device parameters are considered from Predictive Technology Model (PTM). The V-I Characteristics of FinFET is plotted considered at 22nm technology with high-K dielectric. Output characteristics for varying width of HIGH-k FinFET 22nm technology and Inverter Characteristics for 22nm high-k FinFET based Inverter circuit are evaluated and meets its requirements. The gain and phase-margin of OPAMP are identified to be greater than 53dB and 58° respectively. In this work a 1 V Supply is used as an input voltage, the Power dissipation is 12 µ W and the overall performance of OPAMP circuit was improved by 4%.The Power Supply Rejection Ratio (PSRR) is estimated to be around 45dB. UGB of OPMAP is 100GHz, Slew rate is 1V/µs and overshoot is less than 4%.OPAMP is validated considering the response of inverting, noninverting and Comparator.

# Acknowledgement

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6.7.11 using which the schematic capture and simulation results were carried out. We acknowledge PTM.edu for giving us permission to use FinFET model files and access to device parameters for our work. The authors acknowledge the valuable suggestions given by Prof. Cyril Prasanna raj. P. We also thank Dr. Subramanya K N Principal of R V Engineering college and Head of the Department of Electronics and Communication for having permitted us to use the research facilities available in the esteemed college.

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