## Converters with Reduced Duty Cycle Range and Ground Connected to the Positive Input Voltage Terminal

FELIX A. HIMMELSTOSS Faculty of Electronic Engineering and Entrepreneurship, University of Applied Sciences Technikum Wien, Hoechstaedtplatz 6, 1200 Vienna, AUSTRIA

*Abstract:* - A family of converters with reduced duty cycle range is treated here. Two-step-down, two step-up, and four step-up-down converters are investigated. Four different voltage transformation ratios can be found. For all converters, the large signal and the small signal models of the ideal case are given. Furthermore, the connections of the operating point values and the voltage stress across the semiconductors are indicated. Simulations for the steady-state are shown. A method to calculate the transfer functions is proposed and one transfer function for type 1 is shown as an example. The inrush current, when the converter is connected to a stiff input voltage source, is studied with the help of calculations, and time- and phase-diagrams. Several variations and combinations are also shown.

Key-Words: - DC/DC converter, reduced duty cycle, step-up, step-down, step-up-down, inrush current

Received: May 11, 2024. Revised: September 14, 2024. Accepted: November 13, 2024. Published: December 23, 2024.

## **1** Introduction

DC/DC converters are important building blocks in industrial and domestic systems. In addition to the converters described in the textbooks, [1], [2], [3], many other converters have been published. [4], is a concerning comprehensive review step-up converters. In the paper [5] more than a hundred topologies are shown. The original study for the generation and analyses of DC/DC converters is [6]. For three terminal converters [7] is very informative. A basic text concerning DC/DC converters with limited duty cycle range is given in [8]. The duty cycle ratio is lower or higher than onehalf. This can be interesting when snubber networks are used where the recovery time is fixed, or when the interleave concept is used. In these cases, two or more converters are used in parallel and supplied from the same input source feeding the same load. The control signals are shifted by 180 degrees when two converter stages are used or 120 degrees when three stages are used. A second concept to combine two converters is the floating two-stage converter, [9], [10]. For this kind of converter, the now treated converters can be used for the second stage.

## 2 Step-down Converters

Two versions of step-down converters are possible (Figure 1 and Figure 3). Both converters are non-

inverting. To demonstrate the method of the analyzation the converter type 1 is used.



Fig. 1: Type 1: step-down converter I

With ideal devices and continuous mode, one has to describe the circuit with state equations for the two modes, combine them, and linearize them to get the operating point connections and the small signal model. For mode M1, the active switch (the transistor which can be turned on and off, arbitrarily) is turned on, and the passive switch (the diode) is off, one gets the state equations, a set of differential equations:

$$\frac{di_{L1}}{dt} = \frac{-u_{C2} + u_1}{L_1} \tag{1}$$

$$\frac{di_{L2}}{dt} = \frac{u_{C1} - u_{C2}}{L_2} \tag{2}$$

$$\frac{du_{C1}}{dt} = -\frac{i_{L2}}{C_1} \tag{3}$$

$$\frac{du_{C2}}{dt} = \frac{i_{L2} + i_{L2} - u_{C2}/R}{C_2}.$$
 (4)

Now one can combine these four equations into one matrix equation:

$$\frac{d}{dt} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & \frac{1}{L_2} & -\frac{1}{L_2} \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ \frac{1}{L_2} & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} (u_1)^{-1}.$$
(5)

For the second mode, M2 (the electronic switch is off and the diode is on) the state equations are:

$$\frac{di_{L1}}{dt} = \frac{-u_{C1}}{L_1} \tag{6}$$

$$\frac{di_{L2}}{dt} = \frac{-u_1}{L_2} \tag{7}$$

$$\frac{du_{C1}}{dt} = \frac{i_{L1}}{C_1}$$
(8)

$$\frac{du_{C2}}{dt} = \frac{-u_{C2}/R}{C_2} \,. \tag{9}$$

Combination leads to:

$$\frac{d}{dt} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix} (u_1) \cdot (10)$$

When the time constants of the system are large compared to the period of the switching frequency, (5) is multiplied by d and (10) by (1-d) and both are added to obtain the state space model of the converter:

$$\frac{d}{dt} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_1} & -\frac{d}{L_1} \\ 0 & 0 & \frac{d}{L_2} & -\frac{d}{L_2} \\ \frac{1-d}{C_1} & -\frac{d}{C_1} & 0 & 0 \\ \frac{d}{C_2} & \frac{d}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \frac{d}{L_1} \\ \frac{d-1}{L_2} \\ 0 \\ 0 \end{bmatrix} (u_1)^{-1}$$
(11)

This model is also called a large signal model because it is valid as long the converter does not change into the discontinuous mode. The duty cycle is also variable and is multiplied with the state variables  $i_{L1}$ ,  $i_{L2}$ ,  $u_{C1}$ , and  $u_{C2}$  and also with the input

variable  $u_1$ . The large signal model is therefore a nonlinear one. To obtain the transfer functions (c.f. section 5) one has to linearize the equation around an operating point. All variables can be described by a combination of the operating point value (written in capital letters with a zero in the index) and the disturbance around the operating point (written with small letters with a roof on top). The small signal model is therefore:

$$\frac{d}{dt} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} = \begin{pmatrix} 0 & 0 & \frac{D_0 - 1}{L_1} & -\frac{D_0}{L_1} \\ 0 & 0 & \frac{D_0}{L_2} & -\frac{D_0}{L_2} \\ \frac{1 - D_0}{C_1} & -\frac{D_0}{C_1} & 0 & 0 \\ \frac{D_0}{C_2} & \frac{D_0}{C_2} & 0 & -\frac{1}{RC_2} \end{pmatrix} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} + \\ + \begin{pmatrix} \frac{D_0}{L_2} & \frac{U_{C10} - U_{C20} + U_{10}}{L_1} \\ \frac{D_0 - 1}{L_2} & \frac{U_{C10} - U_{C20} + U_{10}}{L_2} \\ 0 & -\frac{I_{L10} + I_{L20}}{C_1} \\ 0 & \frac{I_{L10} + I_{L20}}{C_2} \end{pmatrix} \begin{pmatrix} \hat{u}_1 \\ \hat{d} \end{pmatrix}$$

For the operating point, one gets:

$$(D_0 - 1)U_{C10} - D_0 U_{C20} + D_0 U_{10} = 0$$
(13)

$$D_0 U_{C10} - D_0 U_{C20} + (D_0 - 1) U_{10} = 0$$
 (14)

$$(1 - D_0)I_{L10} - D_0I_{L20} = 0 (15)$$

$$D_0 I_{L10} + D_0 I_{L20} - I_{LOAD} = 0.$$
 (16)

This leads to the connections of the operating point values according to:

$$\frac{U_{C10}}{U_{10}} = 1 \tag{17}$$

$$\frac{U_{C20}}{U_{10}} = \frac{2D_0 - 1}{D_0} \tag{18}$$

$$\frac{I_{L10}}{I_{LOAD}} = 1 \tag{19}$$

$$\frac{I_{L20}}{I_{LOAD}} = \frac{1 - D_0}{D_0} \,. \tag{20}$$

From (18) one can see that the duty cycle must be:  $D_0 \ge 0.5$ . (21)

The steady-state voltage across  $C_1$  is equal to the input voltage. This can be easily obtained by inspecting the circuit diagram and looking at the loop: input voltage  $U_1$ , coil  $L_2$ , capacitor  $C_1$ , coil  $L_1$ . The voltages across the coils are zero in the mean, and therefore the mean voltage across the capacitor  $C_1$  must be equal to the input voltage. The mean current through the first inductor is equal to the load current. From the voltage across the output capacitor  $C_2$  one can see that the duty cycle is limited to values greater than 0.5.

The voltage stress across the semiconductors is given by:

$$U_{S,\max} = -U_2 + U_1 + U_{C1} = -U_2 + 2U_1 = |U_{D,\max}|.$$
(22)

Figure 2 shows a simulation for the steady state: the currents through the coils, the load current, the control signal, the output voltage, and the input voltage. In the simulations of all converters described in this paper, the inductors have the value  $47 \mu$ H and the capacitors 330  $\mu$ F.



Fig. 2: Type 1 up to down: current through L1 (red), load current (brown), current through L2 (violet); control signal (turquoise), output voltage (green), input voltage (blue)

The second possible step-down converter with a reduced duty cycle is shown in Figure 3.



Fig. 3: Type 2: step-down converter II

Just so as shown for type 1 one gets:

$$\frac{d}{dt} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{d}{L_1} & 0 \\ 0 & 0 & \frac{d-1}{L_2} & -\frac{1}{L_2} \\ -\frac{d}{C_1} & \frac{1-d}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \frac{d-1}{L_1} \\ \frac{d}{L_2} \\ 0 \\ 0 \end{bmatrix} (u_1)$$
(23)

$$\frac{d}{dt} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C2} \\ \hat{u}_{C2} \\ u_{C2} \end{pmatrix} = \begin{pmatrix} 0 & 0 & \frac{D_0}{L_1} & 0 \\ 0 & 0 & \frac{D_0 - 1}{L_2} & -\frac{1}{L_2} \\ -\frac{D_0}{C_1} & \frac{1 - D_0}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \\ \end{pmatrix} + \begin{pmatrix} \frac{D_0 - 1}{L_1} & \frac{U_{C10} + U_{10}}{L_1} \\ \frac{D_0}{L_2} & \frac{U_{C10} + U_{10}}{L_2} \\ 0 & 0 \\ 0 & 0 \\ \end{pmatrix} \begin{pmatrix} \hat{u}_1 \\ \hat{d} \\ \hat{d} \\ \end{pmatrix}$$
(24)

The operating point values are equal to those of type 1 (17), (18), (19), (20), but the dynamics have changed and so has the inrush current (cf. section 6). The voltage stress across the semiconductors is equal to the one of type 1.

## **3** Step-up Converters

It is also possible to construct two step-up converters (Figure 4 and Figure 6) with reduced duty cycle and ground on the positive input side. Both converters are non-inverting, which means that input and output voltages have the same polarity.



Fig. 4: Type 3, step-up converter I

With the help of Figure 4 one can immediately see that the voltage across C1 must be equal to the output voltage. The basic results are:

$$\frac{d}{dt} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{d}{L_1} & \frac{d-1}{L_1} \\ 0 & 0 & \frac{d-1}{L_2} & \frac{d}{L_2} \\ -\frac{d}{C_1} & \frac{1-d}{C_1} & 0 & 0 \\ \frac{1-d}{C_2} & -\frac{d}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \frac{1-d}{L_1} \\ \frac{1-d}{L_2} \\ 0 \\ 0 \end{bmatrix} (u_1)$$

$$(25)$$

$$\frac{d}{dt} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{i}_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{D_0}{L_1} & \frac{D_0 - 1}{L_1} \\ 0 & 0 & \frac{D_0 - 1}{L_2} & \frac{D_0}{L_2} \\ -\frac{D_0}{C_1} & \frac{1 - D_0}{C_1} & 0 & 0 \\ \frac{1 - D_0}{C_2} & -\frac{D_0}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} + \\
+ \begin{bmatrix} \frac{1 - D_0}{L_1} & \frac{U_{C10} + U_{C20} - U_{10}}{L_2} \\ \frac{1 - D_0}{L_2} & \frac{U_{C10} + U_{C20} - U_{10}}{L_2} \\ 0 & -\frac{I_{L10} + I_{L20}}{C_1} \\ 0 & -\frac{I_{L10} + I_{L20}}{C_2} \end{bmatrix} \begin{pmatrix} \hat{u}_1 \\ \hat{d} \end{pmatrix}$$
(26)

$$\frac{U_{C10}}{U_{10}} = \frac{U_{C20}}{U_{10}} = \frac{1 - D_0}{1 - 2D_0}$$
(27)

$$\frac{I_{L10}}{I_{LOAD}} = \frac{1 - D_0}{1 - 2D_0} \tag{28}$$

$$\frac{I_{L20}}{I_{LOAD}} = \frac{D_0}{1 - 2D_0} \,. \tag{29}$$

By (27), (28), and (29) one can recognize that the duty cycle must be lower than 0.5

 $D_0 < 0.5$  .

The converter must be driven by a duty cycle smaller than one-half. The voltage stress across the semiconductors is given by:

$$U_{S,\max} = U_{C1} - U_1 + U_2 = 2U_2 - U_1 = |U_{D,\max}|.$$
 (30)

Figure 5 shows the currents through the capacitors, the currents through the inductors, the load current, the control signal, the input voltage, and the output voltage.



Fig. 5: Type 3, up to down: current through C2 (dark violet); current through C1 (grey); current through L1 (red), current through L2 (violet), load current (brown); control signal (turquoise), input voltage (blue), output voltage (green)

The second variant of a step-up converter is shown in Figure 6. One can see that this converter has a continuous input current because of the inductor L1 and that the output voltage is the sum of the input voltage and the voltage across C1.



Fig. 6: Type 4, step-up converter II

The basic results are:

$$\frac{d}{dt} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{d}{L_1} & \frac{d-1}{L_1} \\ 0 & 0 & \frac{d-1}{L_2} & \frac{d}{L_2} \\ -\frac{d}{C_1} & \frac{1-d}{C_1} & 0 & 0 \\ \frac{1-d}{C_2} & -\frac{d}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} (u_1)^{-1} (31)$$

Matrix A is equal to type 3 but the input matrix is different. The small signal model is described by:

$$\frac{d}{dt} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ u_{C1} \\ \lambda_{u22} \end{pmatrix} = \begin{pmatrix} 0 & 0 & \frac{D_0}{L_1} & \frac{D_0 - 1}{L_1} \\ 0 & 0 & \frac{D_0 - 1}{L_2} & \frac{D_0}{L_2} \\ -\frac{D_0}{C_1} & \frac{1 - D_0}{C_1} & 0 & 0 \\ \frac{1 - D_0}{C_2} & -\frac{D_0}{C_2} & 0 & -\frac{1}{RC_2} \end{pmatrix} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ u_{C1} \\ \lambda_{uC1} \\ \lambda_{uC2} \end{pmatrix} + \\
+ \begin{pmatrix} \frac{1}{L_1} & \frac{U_{C10} + U_{C20}}{L_1} \\ 0 & \frac{U_{C10} + U_{C20}}{L_2} \\ 0 & -\frac{I_{L10} + I_{L20}}{C_1} \\ 0 & -\frac{I_{L10} + I_{L20}}{C_2} \end{pmatrix} \begin{pmatrix} \hat{u}_{11} \\ \hat{d} \end{pmatrix}$$
(32)

The operating point values differ compared to the other type, but the converter has the same voltage transformation ratio. The voltage across C1 changes according to:

$$\frac{U_{C10}}{U_{10}} = \frac{D_0}{1 - 2D_0},\tag{33}$$

the other values can be taken from (27), (28), (29). The voltage stress across the semiconductors is equal to the one of type 3.

## **4** Step-up-down Converters

Four different step-up-down converters can be constructed. All four are inverting the input voltage. They have two distinct voltage transformation ratios. The circuit diagram for type 5 is depicted in Figure 7.



Fig. 7: Type 5, step-up-down converter I

The results were obtained in the same way as was shown for type 1 and are:

$$\frac{d}{dt} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_1} & 0 \\ 0 & 0 & \frac{d}{L_2} & -\frac{1}{L_2} \\ \frac{1-d}{C_1} & -\frac{d}{C_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \frac{d}{L_1} \\ \frac{d-1}{L_2} \\ 0 \\ 0 \end{bmatrix} (u_1)$$
(34)

The small signal model has two input variables, the input voltage and the duty cycle:

$$\frac{d}{dt} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{C1} \\ \hat{u}_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{D_0 - 1}{L_1} & 0 \\ 0 & 0 & \frac{D_0}{L_2} & -\frac{1}{L_2} \\ \frac{1 - D_0}{C_1} & -\frac{D_0}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} + \\
+ \begin{bmatrix} \frac{D_0}{L_1} & \frac{U_{C10} + U_{10}}{L_1} \\ \frac{D_0 - 1}{L_2} & \frac{U_{C10} + U_{10}}{L_2} \\ 0 & -\frac{I_{L10} + I_{L20}}{C_1} \\ 0 & 0 \end{bmatrix} \begin{pmatrix} \hat{u}_1 \\ \hat{d} \end{pmatrix} \\
\frac{U_{C10}}{U_{10}} = \frac{D_0}{1 - D_0} \tag{36}$$

$$\frac{U_{C20}}{U_{10}} = \frac{2D_0 - 1}{1 - D_0} \tag{37}$$

$$\frac{I_{L10}}{I_{LOAD}} = \frac{D_0}{1 - D_0}$$
(38)

$$\frac{I_{L20}}{I_{LOAD}} = 1 \tag{39}$$

The duty cycle must be equal to or higher than 0.5:  $D_0 \ge 0.5$  (40)

The voltage stress across the semiconductors is given by:

$$U_{S,\max} = U_1 + U_{C1} = 2U_1 + U_2 = |U_{D,\max}| \qquad (41)$$

Figure 8 depicts the input current, the currents through the coils, the load current, the control signal, and the input voltage. The input current is negative during the off-time of the active switch. So energy is fed back to the input source during this off-time. One can interpret this as analogous to the reactive power in an AC system.



Fig. 8: Type 5, up to down: input current (dark violet); current through L1 (red), current through L2 (violet), load current (brown); output voltage (green), control signal (turquoise), input voltage (blue)

Figure 9 shows the second version with the same voltage transformation ratio. The voltage across C1 must be equal to the input voltage in the steady state.



Fig. 9: Type 6, step-up-down converter II

$$\frac{d}{dt} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{vmatrix} 0 & 0 & \frac{d}{L_1} & \frac{d-1}{L_1} \\ 0 & 0 & \frac{d-1}{L_2} & \frac{d-1}{L_2} \\ -\frac{d}{C_1} & \frac{1-d}{C_1} & 0 & 0 \\ \frac{1-d}{C_2} & \frac{1-d}{C_2} & 0 & -\frac{1}{RC_2} \end{vmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \frac{d-1}{L_1} \\ \frac{d}{L_2} \\ 0 \\ 0 \end{pmatrix} (u_1)$$

$$(42)$$

$$\frac{d}{dt} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{i}_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{D_0}{L_1} & \frac{D_0 - 1}{L_1} \\ 0 & 0 & \frac{D_0 - 1}{L_2} & \frac{D_0 - 1}{L_2} \\ -\frac{D_0}{C_1} & \frac{1 - D_0}{C_1} & 0 & 0 \\ \frac{1 - D_0}{C_2} & \frac{1 - D_0}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} + \\ + \begin{bmatrix} \frac{D_0 - 1}{L_1} & \frac{U_{C10} + U_{C20} + U_{10}}{L_1} \\ \frac{D_0}{L_2} & \frac{U_{C10} + U_{C20} + U_{10}}{L_2} \\ 0 & -\frac{I_{L10} + I_{L20}}{C_1} \\ 0 & -\frac{I_{L10} + I_{L20}}{C_2} \end{bmatrix} \begin{pmatrix} \hat{u}_1 \\ \hat{d} \end{pmatrix}$$
(43)

$$\frac{U_{C10}}{U_{10}} = 1 \tag{44}$$

$$\frac{U_{C20}}{U_{10}} = \frac{2D_0 - 1}{1 - D_0} \tag{45}$$

$$\frac{I_{L10}}{I_{LOAD}} = 1 \tag{46}$$

$$\frac{I_{L20}}{I_{LOAD}} = \frac{D_0}{1 - D_0} \,. \tag{47}$$

From (45) one can recognize that the duty cycle must be higher than 0.5:

$$D_0 \ge 0.5$$
. (48)

The voltage stress across the semiconductors is equal to the one of type 5.

The converter type 7 (Figure 10) has the interesting quality that the input current is continuous. The voltage across the first capacitor is equal to the sum of the input and the output voltages.





$$\frac{d}{dt} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_1} & \frac{d}{L_1} \\ 0 & 0 & \frac{d}{L_2} & \frac{d-1}{L_2} \\ \frac{1-d}{C_1} & -\frac{d}{C_1} & 0 & 0 \\ -\frac{d}{C_2} & \frac{1-d}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} (u_1) \quad (49)$$

$$\frac{d}{dt} \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{D_0 - 1}{L_1} & \frac{D_0}{L_2} \\ \frac{1-D_0}{C_1} & -\frac{D_0}{C_1} & 0 & 0 \\ -\frac{D_0}{C_2} & \frac{1-D_0}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L1} \\ \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L2} \\ u_{C1} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h}_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \hat{h$$

$$\frac{U_{C10}}{U_{10}} = \frac{1 - D_0}{1 - 2D_0} \tag{51}$$

$$\frac{U_{C20}}{U_{10}} = \frac{D_0}{1 - 2D_0} \tag{52}$$

$$\frac{I_{L10}}{I_{LOAD}} = \frac{D_0}{1 - 2D_0}$$
(53)

$$\frac{I_{L20}}{I_{LOAD}} = \frac{1 - D_0}{1 - 2D_0} \,. \tag{54}$$

From the steady-state equations one can see that the duty cycle must be lower than 0.5:

$$D_0 < 0.5$$
. (55)

The duty cycle must be smaller than 0.5. Figure 11 depicts the current through the inductors,

the load current, the output voltage, the control signal, and the input voltage. The voltage stress across the semiconductors is given by

$$U_{S,\max} = U_2 + U_{C1} = U_1 + 2U_2 = |U_{D,\max}|$$
. (56)



Figure 11; Type 7, up to down: current through L2 (violet), current through L1 (red), load current (brown); output voltage (green), control signal (turquoise), input voltage (blue)

Figure 12 shows the fourth possibility to design a step-up-down converter with a reduced duty cycle.



Fig. 12: Type 8, step-up-down converter IV

The linearized model is:

$$\frac{d}{dt} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{D_0 - 1}{L_1} & \frac{D_0}{L_1} \\ 0 & 0 & \frac{D_0}{L_2} & \frac{D_0 - 1}{L_2} \\ \frac{1 - D_0}{C_1} & -\frac{D_0}{C_1} & 0 & 0 \\ -\frac{D_0}{C_2} & \frac{1 - D_0}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} + \\ + \begin{bmatrix} \frac{D_0}{L_1} & \frac{U_{C10} + U_{C20} + U_{10}}{L_1} \\ \frac{D_0}{L_2} & \frac{U_{C10} + U_{C20} + U_{10}}{L_2} \\ 0 & -\frac{I_{L10} + I_{L20}}{C_1} \\ 0 & -\frac{I_{L10} + I_{L20}}{C_2} \end{bmatrix} \begin{pmatrix} \hat{u}_{11} \\ \hat{d} \end{pmatrix}$$

The large signal model is given by:

$$\frac{d}{dt} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_1} & \frac{d}{L_1} \\ 0 & 0 & \frac{d}{L_2} & \frac{d-1}{L_2} \\ \frac{1-d}{C_1} & -\frac{d}{C_1} & 0 & 0 \\ -\frac{d}{C_2} & \frac{1-d}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \frac{d}{L_1} \\ \frac{d}{L_2} \\ 0 \\ 0 \end{bmatrix} (u_1)$$
(58)

The state matrix is equal to the one for type 7.

The connections between the operating point values are equal to those of type 7 except:

$$\frac{U_{C10}}{U_{10}} = \frac{D_0}{1 - 2D_0} \,. \tag{59}$$

The voltage stress across the semiconductors is equal to the one of type 5.

Figure 13 shows the input current, the current through the coils, the load current, the output voltage, the control signal, and the input voltage. The input current is pulsating.



Fig. 13: Type 8, up to down: input current (dark violet); current through L2 (violet), current through L1 (red), load current (brown); output voltage (green), control signal (turquoise), input voltage (blue)

## **5** Transfer Function

Using the simple linear control theory, the transfer functions of the converter must be known. Utilizing abbreviations for the elements of the state matrix and the input matrix:

$$\frac{d}{dt} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & A_{13} & A_{14} \\ 0 & 0 & A_{23} & A_{24} \\ A_{31} & A_{32} & 0 & 0 \\ A_{41} & A_{42} & 0 & A_{44} \end{bmatrix} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} + \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \\ 0 & B_{32} \\ 0 & B_{42} \end{bmatrix} \begin{pmatrix} \hat{u}_{1} \\ \hat{d} \end{pmatrix} \quad (60)$$

( .

and with the Laplace transformation:

$$\begin{bmatrix} s & 0 & -A_{13} & -A_{14} \\ 0 & s & -A_{23} & -A_{24} \\ -A_{31} & -A_{32} & s & 0 \\ -A_{41} & -A_{42} & 0 & s-A_{44} \end{bmatrix} \begin{pmatrix} I_{L1}(s) \\ I_{L2}(s) \\ U_{C1}(s) \\ U_{C2}(s) \end{pmatrix} = \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \\ 0 & B_{32} \\ 0 & B_{42} \end{bmatrix} \begin{pmatrix} U_{1}(s) \\ D(s) \end{pmatrix} \cdot$$
(61)

One can calculate eight transfer functions.

The denominator of all these transfer functions is the determinant of the coefficient matrix and is given by:

$$Den = s^{4} - A_{44}s^{3} - (A_{14}A_{41} + A_{24}A_{42} + A_{13}A_{31} + A_{23}A_{32})s^{2} + A_{44}(A_{13}A_{31} + A_{23}A_{32})s + A_{13}A_{24}A_{31}A_{42} - A_{14}A_{23}A_{31}A_{42} - A_{13}A_{24}A_{32}A_{41} + A_{14}A_{23}A_{32}A_{41}.$$
(62)

The most important numerators are the voltage across the second capacitor (which is the output voltage) in dependence on the duty cycle and on the input voltage. The transfer functions are given by:

$$G_{U2D}(s) = \frac{NUMU2D}{DEN}$$
(63)

$$G_{U2U1}(s) = \frac{NUMU2U1}{DEN}$$
(64)

with

$$NUMU2D = B_{42}s^{3} + (A_{42}B_{22} + A_{41}B_{12})s^{2} + \begin{pmatrix} -A_{23}A_{32}B_{42} \\ -A_{13}A_{31}B_{42} + A_{23}A_{42}B_{32} + A_{13}A_{41}B_{32} \end{pmatrix}s^{+} (65) (A_{13}A_{31}A_{42}B_{22} - A_{13}A_{31}A_{41}B_{22} - A_{23}A_{31}A_{42}B_{12} + A_{23}A_{32}A_{41}B_{12}) NUMU2U1 = (A_{42}B_{12} + A_{41}B_{11})s^{2} - A_{13}A_{31}A_{42}B_{12} + A_{13}A_{32}A_{41}B_{12} + . (66) + A_{23}A_{31}A_{42}B_{11} - A_{23}A_{32}A_{41}B_{11}$$

Figure 14 shows the Bode plot between the output voltage and the duty cycle, of a converter of type 1. One can see the two resonances caused by the two conjugate complex pole pairs and a complex zero which must have a positive real part because these zeros also shift the phase by minus 180 degrees. The third zero has a negative real part and shifts the phase up again by 90 degrees.



Fig. 14: Bode plot between output voltage and duty cycle: solid line: gain, dotted line: phase

## 6 Inrush Current

A very important topic is the inrush current when the converter is connected to a stable input voltage source such as batteries or a stiff DC grid. In this section, the basics are described. The inductors are taken as constant. In practice, they will probably saturate and their value will decrease. The inrush current will therefore be higher. For the calculation, the saturated inductor value can be used in this case.

#### **6.1** Type 1 (Figure 1)

The output is decoupled by the switch. The inrush current is described by:

$$U_1 = \left(L_1 + L_2\right) \frac{di_{IN}}{dt} + \frac{1}{C_1} \int_0^t i_{IN} dt$$
 (67)

Leading to an inrush current of the undamped resonant circuit:

$$i_{IN} = U_1 \sqrt{\frac{C_1}{(L_1 + L_2)}} \sin\left(\sqrt{\frac{1}{C_1(L_1 + L_2)}}t\right).$$
 (68)

Due to parasitic resistors, this ringing is damped and is shown as a diagram with the voltage across C1 in the horizontal direction and with the current through both inductors in the vertical direction (Figure 15). The final value of the voltage across C1 is equal to the input voltage and the currents through the coils are zero.



Fig. 15: Type 1: inrush

#### 6.2 Type 2 (Figure 3)

The resonant circuit which produces the inrush consists of the series connection of the two coils and the two capacitors and is described by:

$$U_1 = (L_1 + L_2) \frac{di_{IN}}{dt} + \frac{C_1 + C_2}{C_1 C_2} \int_0^t i_{IN} dt$$
(69)

Leading to:

$$i_{IN} = U_1 \sqrt{\frac{C_1 C_2}{(L_1 + L_2)(C_1 + C_2)}} \sin\left(\sqrt{\frac{(C_1 + C_2)}{C_1 C_2(L_1 + L_2)}}t\right).$$
(70)

Figure 16 shows the damped inrush current.



#### 6.3 Type 3 (Figure 4)

The diode allows only one half-period of the inrush current. A small ringing occurs between the inductors and the capacitors, but this does not influence the input source. Figure 17 shows the currents through the diode and the coils.



Fig. 17: Type 3, up to down: input current (red), current through L1 (blue), current through L2 (green)

The calculation of the inrush peak through the diode is very simple. With constant input voltage U1 connected to the circuit, two currents through the two series-resonant circuits occur. For the current of the first resonant circuit, one can use the differential-integral equation:

$$U_1 = L_2 \frac{di_{L2}}{dt} + \frac{1}{C_1} \int_0^t i_{L2} dt$$
(71)

Leading to:

$$i_{L2} = U_1 \sqrt{\frac{C_1}{L_2}} \sin\left(\sqrt{\frac{1}{C_1 L_2}}t\right).$$
 (72)

A similar equation can be written for the second resonance circuit (L1, C2) leading to a current peak of

$$\hat{I}_{IN} = U_1 \left( \sqrt{\frac{C_1}{L_2}} + \sqrt{\frac{C_2}{L_1}} \right).$$
(73)

#### 6.4 Type 4 (Figure 6)

When the input voltage is applied to the converter, D1 turns on and during this time the inrush current, which is equal to the current through L1, is described only by:

$$U_1 = L_1 \frac{di_{L1}}{dt} + \frac{1}{C_2} \int_0^t i_{L1} dt$$
 (74)

Leading to:

$$i_{L2} = U_1 \sqrt{\frac{C_2}{L_1}} \sin\left(\sqrt{\frac{1}{C_2 L_1}}t\right).$$
 (75)

This equation is only valid as long as the diode is conducting. The characteristic impedance of the resonant circuit Z=0.378  $\Omega$  leads to the inrush peak value:

$$\hat{I}_{IN} = \hat{I}_{L1} = 64 \text{ A}$$
 (76)

The peak value of the simulation is a little bit lower because of the parasitic resistors and due to a small current through C1 and L2 because of the onward voltage of the diode.

Approximately, after a one-half period the diode turns off and both capacitors and both coils are in series. Now the inrush current is described by (the load resistor is omitted):

$$U_1 = \left(L_1 + L_2\right) \frac{di_{IN}}{dt} + \frac{C_1 + C_2}{C_1 C_2} \int_0^t i_{IN} dt$$
(77)

Leading to:

$$i_{IN} = U_1 \sqrt{\frac{C_1 C_2}{(L_1 + L_2)(C_1 + C_2)}} \sin\left(\sqrt{\frac{(C_1 + C_2)}{C_1 C_2(L_1 + L_2)}}t\right).$$
(78)

The characteristic impedance is reduced to:

$$Z = \sqrt{\frac{(L_1 + L_2)(C_1 + C_2)}{C_1 C_2}}$$
(79)

Leading to:

Z=0.75 Ω,  $\hat{I}_{IN}$  = 32 A, ω=8030 s<sup>-1</sup>, f=1278 Hz, T=783 µs The damping is produced by the parasitic resistors and the applied load.



Fig. 18: Type 4, up to down: current through the diode (dark violet); inrush current (red)



Fig. 19: Type 4, inrush current (red) drawn over the output voltage

With the help of a phase diagram (Figure 19), the complete inrush is depicted.

Figure 18 shows the current through D1 and the current through L1 which is equal to the inrush current at the beginning.

#### 6.5 Type 5 (Figure 7)

The inrush current which is equal to the current through L1 is described by:

$$U_1 = \left(L_1 + L_2\right) \frac{di_{IN}}{dt} + \frac{C_1 + C_2}{C_1 C_2} \int_0^t i_{IN} dt$$
(80)

Leading to:

$$i_{IN} = U_1 \sqrt{\frac{C_1 C_2}{(L_1 + L_2)(C_1 + C_2)}} \sin\left(\sqrt{\frac{(C_1 + C_2)}{C_1 C_2(L_1 + L_2)}}t\right).$$
 (81)

The output voltage and the inrush current after turning on are shown in Figure 20 and also a phase diagram between these two signals is given in Figure 21. The final value is zero for both variables.



Fig. 20: Type 5, up to down: output voltage (green), input voltage (blue); inrush current (red)



Fig. 21: Type 5, inrush current (red) drawn over the output voltage

#### 6.6 Type 6 (Figure 9)

The output is decoupled by the diode. The inrush current is described by:

$$U_1 = \left(L_1 + L_2\right) \frac{di_{IN}}{dt} + \frac{1}{C_1} \int_0^t i_{IN} dt$$
(82)

Leading to:

$$i_{IN} = U_1 \sqrt{\frac{C_1}{(L_1 + L_2)}} \sin\left(\sqrt{\frac{1}{C_1(L_1 + L_2)}}t\right).$$
 (83)

In Figure 22 the inrush current and the input and output voltages are shown. There is no influence on the output (and therefore across the load).



Fig. 22: Type 6, up to down: inrush current (dark violet); output voltage (green), input voltage (blue)

#### 6.7 Type 7 (Figure 10)

When the input voltage is applied to the converter, D1 turns on and at the beginning, the inrush current, which is equal to the current through L1, is described only by:

$$U_1 = L_1 \frac{di_{L1}}{dt} + \frac{1}{C_1} \int_0^t i_{L1} dt$$
 (84)

Leading to:

$$i_{L2} = U_1 \sqrt{\frac{C_2}{L_1}} \sin\left(\sqrt{\frac{1}{C_2 L_1}}t\right).$$
 (85)

This equation is only valid as long as the diode is conducting. The characteristic impedance of the resonant circuit Z=0.378  $\Omega$  leads to the inrush peak value  $\hat{I}_{IN} = \hat{I}_{L1} = 64$  A.

The peak value of the simulation is a little bit lower because of the parasitic resistors and a small current through C2 and L2 and due to the onward voltage of the diode.

Approximately, after a one-half period the diode turns off and both capacitors and both coils are in series. Now the inrush current is described by (the load resistor is omitted)L

$$U_1 = \left(L_1 + L_2\right) \frac{di_{IN}}{dt} + \frac{C_1 + C_2}{C_1 C_2} \int_0^t i_{IN} dt$$
(86)

Leading to:

$$i_{IN} = U_1 \sqrt{\frac{C_1 C_2}{(L_1 + L_2)(C_1 + C_2)}} \sin\left(\sqrt{\frac{(C_1 + C_2)}{C_1 C_2(L_1 + L_2)}}t\right).$$
(87)

The characteristic impedance is changed to:

$$Z = \sqrt{\frac{(L_1 + L_2)(C_1 + C_2)}{C_1 C_2}} .$$
(88)

The damping is produced by the parasitic resistors and the applied load. The phase diagram

current through L1, which is equal to the inrush current over the output voltage is shown in Figure 23.



Fig. 23: Type 7, inrush current (red) drawn over the output voltage

#### 6.8 Type 8 (Figure 12)

No inrush can occur because of the position of the electronic switch.

## 7 Further Modifications

## 7.1 Floating Two-Stage Converters

The concept is shown for type 1. The converter type 1 (Figure 1) is combined with another converter, where the reference is the negative input terminal (Figure 24). The control signals are shifted by 180 degrees.



Fig. 24: Two-stage floating converter with limited duty cycle type 1

Figure 25 shows the input current, the currents through the coils L12 and L22 of stage 2, the currents through the coils L11 and L21 of stage 1, the input voltage, the voltage across one output

capacitor, the control signal of S2, the output voltage, and the control signal of S1. The frequency of the input current is doubled.



Fig. 25: Two-stage floating converter with limited duty cycle type 1: up to down: input current (dark violet); currents through the coils of stage 2 L12 (grey), L22 (light brown); currents through the coils of stage 1 L11 (red), L21 (violet); input voltage (blue), voltage across output capacitor (dark blue), control signal of S2 (dark green, shifted), output voltage (green), control signal of S1 (turquoise)

## 7.2 Interleaved Converter

As an example, two converters according to type 1 are combined. The circuit diagram is given in Figure 26.



Fig. 26: Two-stage interleaved converter with limited duty cycle type 1

The inputs and the outputs of the converters are connected in parallel. This concept is useful for higher-power applications. When the control signals of the two stages are shifted by 180 degrees, the input frequency is doubled. When three converters are used in parallel, the control signals have to be shifted by 120°. Using n converter stages the control signals are shifted by 360°/n. The input current is smoothed. For partial load, not all converters have to be in operation and those used will work with higher efficiency. Figure 27 shows the input current, the currents through the coils of stage 2 L12 and L22, the currents through the coils of stage 1 L11 and L21, the control signal of S2, the control signal of S1, the output voltage, and the input voltage.



Fig. 27: Two-stage interleaved converter with limited duty cycle type 1, up to down: input current (dark violet); currents through the coils of stage 2 L12 (light brown), L22 (grey); currents through the coils of stage 1 L11 (red), L21 (violet); control signal of S2 (dark green, shifted), control signal of S1 (turquoise), output voltage (green), input voltage (blue)

## 7.3 Modified Converter

Other interesting converters can be found when the position of the output capacitor is changed and connected between input and output. This is again shown for the converter type 1 in Figure 28.



Fig. 28: Modified limited duty cycle converter type 1

The input current is now continuous, the voltage stress across the capacitor is changed, and the inrush current is also modified.

## 8 Conclusion

Eight DC/DC converters were investigated. Two of them are step-down, two of them are step-up, and four of them are step-up-down converters. All of them have the following features:

- The reference is the positive input voltage terminal
- The duty cycle is larger or smaller than one-half
- They can be combined to form interleaved converters

Other interesting features can be found:

- Continuous input current (type 4, 7)
- No inrush current (type 8)
- Input current with small energy feedback phases (type 1, 2, 5, and 6)
- Pulsed input current (type 3, 8)
- Continuous output current (type 2, 5)

The converters are useful when the reference point must be positive. This is typical of communication circuits and of electrochemical applications. The converters can easily be combined with another converter, where the reference is the negative input terminal to form a floating two-stage converter. The combination of two or more converters to form interleaved converters are also an interesting application.

#### References:

- [1] F. Zach, *Leistungselektronik*, Frankfurt: Springer, 6th edition 2022 (Text in German).
- [2] N. Mohan, T.Undeland, & W. Robbins, *Power Electronics, Converters, Applications and Design*, New York: W. P. John Wiley & Sons.
- [3] Y. Rozanov, S. Ryvkin, E. Chaplygin, P. Voronin, *Power Electronics Basics*, CRC Press.
- [4] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications, *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143-9178, Dec. 2017, doi: 10.1109/TPEL.2017.2652318.
- [5] B. W. Williams, Generation and Analysis of Canonical Switching Cell DC-to-DC Converters, *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 329-346, Jan. 2014, doi: 10.1109/TIE.2013.2240633.
- [6] S. Cuk, General topological properties of switching structures, *IEEE Power Electronics Specialists Conference*, San Diego, CA, USA, 1979, pp. 109-130, doi: 10.1109/PESC.1979.7081016.

- [7] R. Marquez and M. A. Contreras-Ordaz, The Three-Terminal Converter Cell, Graphs, and Generation of DC-to-DC Converter Families, *IEEE Transactions on Power Electronics*, Vol. 35, No. 8, pp. 7725-7728, Aug. 2020, doi: 10.1109/TPEL.2020.2964700.
- [8] F. A. Himmelstoss, Fourth order DC-DC converters with limited duty cycle range, Proceedings of Intelec 93: 15th International Telecommunications Energy Conference, Paris, France, 1993, pp. 358-364 vol.1, doi: 10.1109/INTLEC.1993.388498.
- [9] D. Coutellier, V. G. Agelidis, S. Choi, Experimental verification of floating-output interleaved-input DC-DC high-gain transformer-less, converter topologies. *IEEE Power Electronics Specialists Conference*, Rhodes, Greece, 2008, pp. 562-568. doi: 10.1109/PESC.2008.4591989.
- [10] P. Lin, W. Jiang, J. Wang, D. Shi, C. Zhang, P. Wang, Toward Large-Signal Stabilization of Floating Dual Boost Converter-Powered DC Microgrids Feeding Constant Power Loads, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 1, pp. 580-589, Feb. 2021. doi: 10.1109/JESTPE.2019.2956097.

#### Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The author contributed to the present research, in all stages from the formulation of the problem to the final findings and solution.

## Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

No funding was received for conducting this study.

#### **Conflict of Interest**

The author has no conflicts of interest to declare.

# Creative Commons Attribution License 4.0 (Attribution 4.0 International, CC BY 4.0)

This article is published under the terms of the Creative Commons Attribution License 4.0 https://creativecommons.org/licenses/by/4.0/deed.en US