A Closed-form Delay Estimation Model for Current-mode High Speed VLSI Interconnects

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Abstract: Closed-form model for the delay estimation of current-mode Resistance Inductance Capacitance (RLC) interconnects in VLSI circuits is presented. The existing Eudes model for interconnect transfer function approximation is extended and applied for further accurate estimation of delay. With the equivalent lossy interconnect transfer function, finite ramp responses are obtained and line delay is estimated for various line lengths, per unit length inductances and load capacitances. The estimated delay values of extended Eudes model are compared with the existing Eudes model against HSPICE W-element model. The obtained delay values of Eudes model worst-case error percentage is 14.3% whereas our extended Eudes model is in good agreement with those of HSPICE results within 2% for the line lengths of 1mm to 10mm.

Keywords: Delay, ramp input, Eudes model, RLC interconnects, MacLaurin series, transient analysis, transfer function, SOC.

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1. Introduction

Advancement in technology leads to chip size reduction and increased on-chip interconnection complexity. The performance improvement by using traditional modeling methods [1]-[4] in future technologies is not beneficial. To reach the speed requirement of VLSI circuits at future technology nodes demands for alternative signaling technique that provides an attractive solution to some of the disputes caused by aggressive interconnect scaling. As per the paper [5], the conventional voltage-mode signaling is not able to meet the speed requirements of future technology generations. So, current-mode signaling has been investigated as a substitute for high speed data transmission over interconnects.

Signaling in global lines is a major bottleneck in high performance VLSI systems due to the dominant limitation of signal propagation delays as compared to circuit delays. So, accurate and efficient delay estimation models are required in current-mode signaling. Accurate estimation of propagation delay in global interconnects plays a predominant role in the early design stages of VLSI systems as compared to local interconnect delays because, global wires supports main functions like clock, signal distribution between the functional blocks and provides power/ground to all functions on a chip.

Starting from lumped RC model to distributed RLC model, various techniques [6]-[8] based on analytical closed-form formulations have been proposed to model delay in voltage-mode interconnects. Similarly for current-mode RC interconnects, closed-form delay analysis model was presented in [9] and the analysis does not include the fast edge input response. In [10] closed-form delay model for distributed current-mode RC line is presented, which included the practical fast edge input response issue but this model could not include the inductance effect in current-mode interconnect. A delay estimation model [11], which is derived using the concept of absorbing inductance effect into equivalent RC model, then modified nodal analysis (MNA) was used.

Various closed-form delay models [9]-[13] for on-chip interconnects in current-mode signaling have more inaccuracy in terms of delay estimation. This paper presents a closed-form delay estimation model for current-mode on-chip RLC interconnects by using the existing Eudes model [14], which was basically for modeling of PCB RLCG interconnects. But, in this paper we have implemented Eudes model and extended Eudes model for current-mode RLC interconnects and are compared against standard HSPICE tool. At deep sub micron VLSI designs Conductance effect can be ignored so, we implemented Eudes model and its extension for RLC interconnects. These mathematical models are implemented in MATLAB for easy of analysis. These models are validated under different ranges of parameters and compared with respect to HSPICE tool.

According to signaling point of view, both voltage and current-mode driver circuits can be approximated by a voltage source and a linear resistance. As compared to voltage-mode receiver circuits, current-mode receiver circuits provide a low-impedance path, so a resistive and parallel low capacitive path is needed at the receiver. Therefore, for sensing a current-mode signal, low input impedance receiver termination is required, which provides current path to ground.

The remainder of the paper is organized as follows. Section II briefly describes the Eudes model and extension of Eudes model for the analysis of current-mode RLC interconnects. Section III reports the validation of the presented models and the results are compared with standard HSPICE. Conclusions and future scope appear at the end.

2. Analysis of Current-mode Rlc Interconnect Using Eudes Model and Its Extension

The analysis of on-chip current-mode RLC interconnects begins with Telegraphers equation in frequency domain. All the closed-form RLC interconnects models assume quasi-TEM mode of signal propagation. The Telegrapher's equations are a pair of linear partial differential equations which illustrate the voltage and current on a transmission line with distance and time as transmission line variables.

The solution of interconnects are described by telegrapher's equations as

$$\frac{\partial}{\partial x}V(z,s) = -(R+sL)I(z,s)$$
$$\frac{\partial}{\partial x}I(z,s) = -sCV(z,s) \quad (1)$$

where 's' is the Laplace-transform variable, z is a variable which represents position; $V(z,s)$ and $I(z,s)$ stand for the voltage and current vectors of the transmission line, respectively, in the frequency domain; and R, L and C are the per unit length (p.u.l.) resistance, inductance, and capacitance matrices, respectively.

The solution of (1) can be written as an exponential matrix function as

$$\begin{bmatrix} V(d,s) \\ -I(d,s) \end{bmatrix} = e^{\phi d}\begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix} \quad (2)$$

where

$$\phi = \begin{bmatrix} 0 & -Z \\ -Y & 0 \end{bmatrix}$$

In (2) 'd' is the length of the transmission line, with Z=R+sL and Y=sC. The exponential matrix of (2) can be written in terms of cosh and sinh functions as

$$e^{\phi d} = \begin{bmatrix} \cosh\left(d\sqrt{ZY}\right) & -Y_0^{-1}\sinh\left(d\sqrt{YZ}\right) \\ -Y_0\sinh\left(d\sqrt{YZ}\right) & \cosh\left(d\sqrt{YZ}\right) \end{bmatrix} \quad (3)$$

where

$$Y_0 = Y(\sqrt{YZ})^{-1}$$

2.1 Eudes Model [14]

This model was developed for the characterization of RF/digital PCB RLCG interconnections for the prediction of the high-speed signal transient responses. This model considers the second order MacLaurin series approximation of the interconnection RLCG-model transfer matrix and the transient responses obtained from the resulting interconnection system transfer function. We applied this model to current-mode RLC interconnects and obtained the delay estimation.

The direct time domain representation of (2) is not possible, so it is difficult to analytically estimate the delay of interconnects. This equation can be realized by applying the second order MacLaurin series for each element of the transfer matrix. The resultant is derived as

$$H(s) = \begin{bmatrix} 1+\frac{Z.Y}{2} & -Z \\ -Y & 1+\frac{Z.Y}{2} \end{bmatrix} \quad (4)$$

A single current-mode RLC line is shown in Fig. 1. The line is driven by a step input and 1-V finite ramp with rise time of 0.1 ns. Current-mode interconnect driver is modeled similar to voltage-mode driver equivalent series resistance R_s but the main difference is with current-mode interconnect receiver, which is modeled as a resistor R_L in parallel with capacitive load C_L for low impedance path which enhances high speed data transmission over longer lines

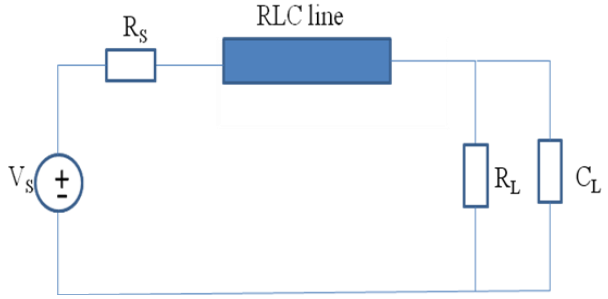

Fig. 1.Equivalent circuit model of the current-mode single line RLC interconnect.

The transfer function matrix in (4) denotes the approximation model of Transmission line without source and load impedances. As per Fig. 1, the source and load impedances matrices need to be cascaded with second order interconnect transfer function to find the complete circuit transfer function

$$H1(s) = \begin{bmatrix} 1 & R_s \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} 1+\frac{Z.Y}{2} & -Z \\ -Y & 1+\frac{Z.Y}{2} \end{bmatrix} * \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_l} & 1 \end{bmatrix} \quad (5)$$

where

$$Z_l = \left(\frac{R_L}{R_L.sC_L+1}\right)$$

The Z_l is an equivalent load impedance of line and is represented as parallel combination of load resistance R_L and C_L.

The frequency domain transfer function at the far end is

$$H1_{11}(s)=\left(\frac{1}{\left(1+\frac{ZY}{2}+R_sY\right)+\frac{1}{Z_l}\left(Z+R_s\left(1+\frac{ZY}{2}\right)\right)}\right) \quad (6)$$

Based on the ABCD parameter model matrix and their expansion leads to the voltage transfer function (6) in frequency domain which can be inverse Laplace transformed to get the time domain response for the estimation of delay.

The equation (6) is the result of Eudes model which approximates current-mode RLC interconnect transfer function model using second order MacLaurin series. But this model has less accuracy so, we extended his work with fourth order MacLaurin series for better accuracy and mathematical analysis is implemented in MATLAB.

2.2 Extended Eudes Model

We have extended the existing Eudes model and obtained an efficient model for current-mode RLC interconnects to get the accurate delay estimation. This model is compared with existing Eudes model and HSPICE and found that our model is having good accuracy at cost of slight increase in computation time

The complicated form (2) is realized by applying Extended Eudes model and is given as

$$H(s)=\begin{bmatrix}1+\frac{ZY}{2}+\frac{(ZY)^2}{24} & -\left(Z+\frac{Z^3}{6}\right)\\ -\left(Y+\frac{Y^3}{6}\right) & 1+\frac{ZY}{2}+\frac{(ZY)^2}{24}\end{bmatrix} \quad (7)$$

The complete transfer function matrix obtained using cascade of source, above interconnect matrix (7) and load impedances matrices is written as H2(s)

$$H2(s)=\begin{bmatrix}1 & R_s\\ 0 & 1\end{bmatrix}\begin{bmatrix}1+\frac{ZY}{2}+\frac{(ZY)^2}{24} & -\left(Z+\frac{Z^3}{6}\right)\\ -\left(Y+\frac{Y^3}{6}\right) & 1+\frac{ZY}{2}+\frac{(ZY)^2}{24}\end{bmatrix}\begin{bmatrix}1 & 0\\ \frac{1}{Z_l} & 1\end{bmatrix} \quad (8)$$

After multiplication of above matrices leads to frequency domain voltage transfer function $H_{11}2(s)$ as first term, written as

$$\left(\frac{1}{1+\frac{ZY}{2}+\frac{(ZY)^2}{4}+R_s\left(Y+\frac{Y^3}{6}\right)+\frac{1}{Z_l}\left[\left(Z+\frac{Z^3}{6}\right)+R_s\left(1+\frac{ZY}{2}+\frac{(ZY)^2}{24}\right)\right]}\right) \quad (9)$$

These transfer function models $H_{11}1(s)$ and $H_{11}2(s)$ of Eudes and extended Eudes model are inverse Laplace transformed using MATLAB to get time domain responses and estimation of delay.

3. Simulation Results

The single current-mode RLC line is presented in this section to demonstrate the validity and efficiency of the proposed method. The results were obtained using MATLAB R2010a operating on HP 64-bit Intel i5 processor with clock speed of 2.53 GHz and are also compared with HSPICE using the W-element method.

The typical interconnect parameters [11] considered for simulation of single current-mode RLC interconnect are given in table-I. The Eudes model and its extended model are implemented in MATLAB for the same set of input parameters.

Table 1. Interconnects parameter for model validation [11]

Unit-length Inductance	Unit-length Capacitance	Unit-length Resistance	R_L	C_L
400nH/m-100nH/m	50pF/m-100pF/m	20k Ω/m-40k Ω/m	10 Ω-10kΩ	10fF-600fF

We considered the rise time of the ramp input signal is 0.1ns, so the maximum frequency necessitated for the presented models responses have been approximated of about 3.5GHz from (10). In order to demonstrate the adaptableness of the proposed modeling method, we varied line lengths, line inductance and load capacitance and observed the delay statistics.

$$f_{max}=\frac{0.35}{t_r} \quad (10)$$

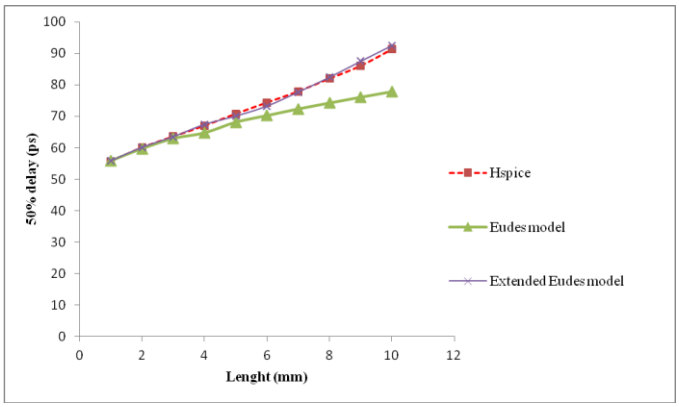

Fig 2. 50% delay versus Line length for various models

As per the data in Fig. 2, it is apparent that as the line length increases from 1mm to 10mm range of SOC global line applications, the delay increases and various models (HSPICE, Eudes and extended Eudes model) delay plots are cascaded. As per calculations of delay, the Eudes model has maximum error percentage of 14.3% whereas extended Eudes model

matches very well with HSPICE and the maximum error percentage is 1.26% for the line length of 10mm. However, for shorter lines (0.3cm) and lower, all the models matches to that of HSPICE with acceptable error percentage within 1%, but for longer lengths the extended Eudes model plays a prominent role in estimating the accurate delay of current-mode interconnect.

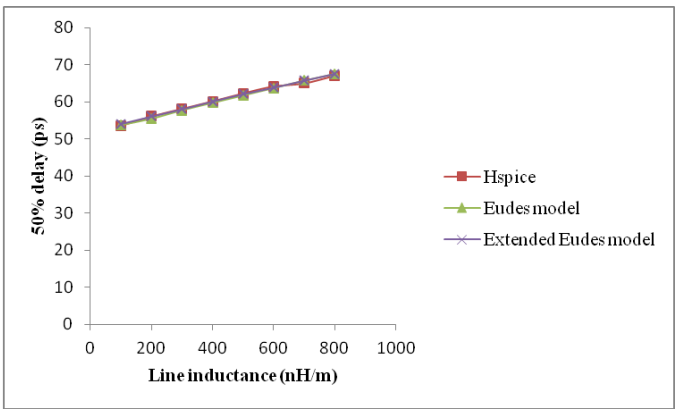

Fig 3. 50% delay versus line inductance for 0.2cm long line

In Fig. 3 there is a clear trend of increasing delay for various per unit length Line inductances of the range 100nH/m to 800nH/m. As observed that, both the presented models give acceptable error percentage of within 1% for the line length of 0.2cm.

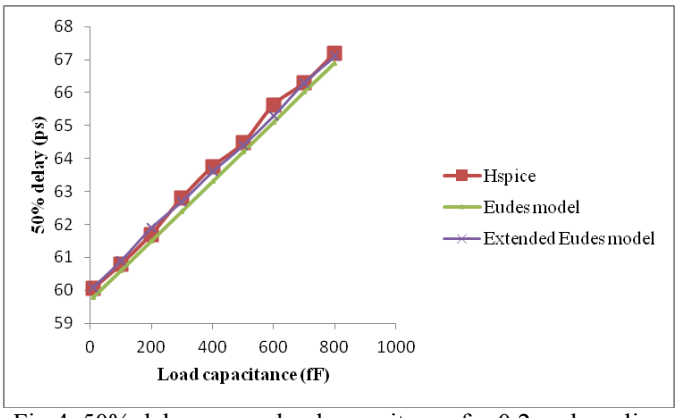

Fig 4. 50% delay versus load capacitance for 0.2cm long line

Fig. 4 depicts the 50% delay values for various interconnect load capacitances in the range of 10fF to 800fF. It can be observed from Fig. 4 that, the delay values of Eudes model deviates with HSPICE but, the extended Eudes model nicely matches with HSPICE and gives acceptable error percentage with in 0.2% for the line length of 0.2cm.

To find the longer line response we increased the length of the line from 0.2cm to 1cm along with variations in line inductances and load capacitances. Figures 5 and 6 are the plots of 50% delay values for line inductance and load capacitance variations at longer length of 1cm.

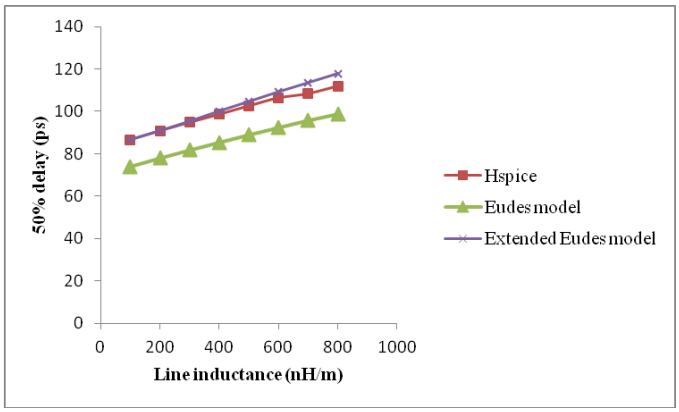

Fig 5. 50% delay versus line inductance for 1cm long line

As shown in Fig. 5 the Eudes model has maximum error percentage of 14.6% whereas the extended Eudes model maximum error percentage is of 5%. It can be noticed that, the extended Eudes model matches with HSPICE until 600nH/m with an error percentage of 2% for the line length of 1cm.

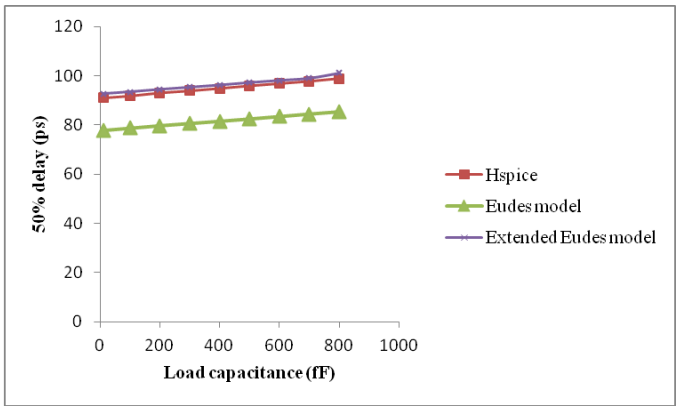

Fig 6. 50% delay versus load capacitance for 1cm long line

Further analysis in Fig. 6 shows that, for 1cm long line with various capacitive loads, the existing Eudes model fall short of to estimate the delay accurately with maximum error percentage of 14.4% but, the extended Eudes model has maximum error percentage of 2.3% and matches with HSPICE, independent of interconnect load capacitance variations.

To find the interaction between the line length values and delay, we varied the values of the per unit length inductance in the Figures 3 & 5 for line lengths of 0.2cm and 1cm. Similarly to find the effect of line length on delay for various models, we varied the value of the capacitive load in the Figures 4 & 6 for 0.2cm and 1cm lines. For both of these cases transient responses were found using HSPICE, Eudes model and its extension model to find the delay of line under various interconnect parametric variations. The extended Eudes model has good accuracy at the cost of slightly higher computation time. These models produce stable results under various interconnect parameters.

4. Conclusion

This paper presents Eudes model and an extension of Eudes model based closed form models for delay estimation of current-mode high speed VLSI interconnects. The purpose of the current study is to estimate the delay of current-mode VLSI interconnects and to find the interaction between delay for various lengths, line inductances and load capacitances using existing Eudes model and its extension against HSPICE tool. This research has shown that, the existing Eudes model fall short of to give good accuracy for longer lines (>0.3cm) but, our extended model is better at longer lines. A single line interconnect has been used for validating the presented models (Eudes model and extended Eudes model) by comparing with the HSPICE. In SOC (system on chip) applications, for global lines of lengths 0.3 cm and below both methods matches nicely with HSPICE but, above 0.3cm length the extended Eudes model is found to be more accurate than existing method. The present study confirms previous findings and contributes additional extension that suggests, for longer lines existing Eudes model underestimates the delay with large error percentage but, extended Eudes model is having better accuracy. These methods can be used to estimate the signal integrity characteristics of Carbon nano tubes.

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