A Generalized Scalar Pwm Approach for Three-phase Voltage-source Inverter Fed Ac Drive

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Abstract: The generalized scalar pulse width modulation (PWM) approach, which unites the conventional PWM methods and most recently developed reduced common mode voltage PWM methods under one umbrella, is established. Through a detailed example, the procedure to generate the pulse patterns of these PWM methods via the generalized scalar PWM approach is illustrated. With this approach, it becomes an easy task to program the pulse patterns of various high performance PWM methods and benefit from their performance in modern three-phase, three wire voltage-source inverters for applications such as motor drives, PWM rectifiers, and active filters. The theory is verified by laboratory experiments. Easy and successful implementation of various high-performance PWM methods is illustrated for a motor drive.

Keywords: Carrier, common-mode voltage, discontinuous PWM (DPWM), generalized scalar PWM, inverter, modulation, near state PWM (NSPWM), pulse width modulation (PWM), PWM implementation, scalar, space vector, space vector PWM (SVPWM), zero sequence.

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1. Introduction

THREE-PHASE, three-wire voltage-source inverters (VSI) are widely utilized in ac motor drive and utility interface applications requiring high performance and high efficiency. In Fig. 1, the standard three-phase two-level VSI circuit diagram is illustrated. The classical VSI generates ac output voltage from dc input voltage with required magnitude and frequency by programming high-frequency rectangular voltage pulses. The carrier-based pulse width modulation (PWM) technique is the preferred approach in most applications due to the low-harmonic distortion waveform characteristics with well-defined harmonic spectrum, fixed switching frequency, and implementation Simplicity. Carrier-based PWM methods employ the "per-carrier cycle volt-second balance" principle to program a desirable inverter output voltage waveform .In every PWM cycle, the reference voltage, which is fixed over the PWM cycle, corresponds to a fixed volt-second value. According to the volt-second balance principle, the inverter output voltages made of rectangular voltage pulses must result in the same volt-seconds as this reference volt-second value. There are two main implementation techniques for carrier based PWM methods: 1) scalar implementation and 2) space vector implementation.

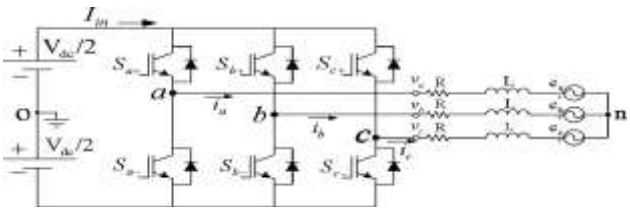

Fig. 1. Circuit diagram of a PWM-VSI drive connected to an R-L-E type load.

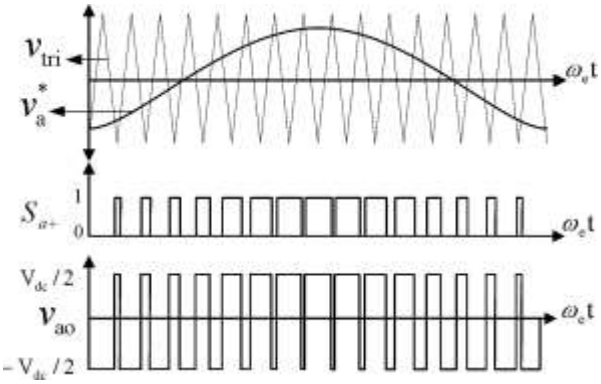

Fig. 2. Triangle intersection PWM phase "*a*" modulation wave *v*a* , switching signal and *va o* voltage.

In the scalar approach, as shown in Fig. 2, for each inverter phase, a modulation wave is compared with a triangular carrier wave [using analog circuits or digital hardware units (PWM units) as conventionally found in motor control microcontroller or DSP chips] and the intersections define the switching instants for the associated inverter leg switches. The mathematics involved in the scalar method modulation waves and the space vector calculations is related. With proper modulation waves, the scalar and space vector PWM pulse patterns can be made identical. Thus, both techniques may have equivalent performance results. But the scalar approach is simpler than the space vector approach from the implementation perspective as the involved computations are generally fewer and less complex .Based on the scalar or vector approach, there are various PWM methods proposed in the literature which differ in terms of their voltage linearity range, ripple voltage/current, switching losses, and high-frequency common mode voltage/current properties. However, the implementation of these methods is not easy and not reported in the literature to sufficient depth.

Furthermore, the relation between the conventional and recently developed reduced CMV (RCMV) PWM methods is not well understood both in terms of implementation characteristics and performance characteristics. Therefore, difficulties arise in implementing and understanding the performance attributes of these PWM methods. This paper first reviews the PWM principles and establishes a general scalar approach that treats the conventional and RCMV–PWM methods, and unites most methods under one umbrella. The paper then reviews the pulse patterns and performance of the popular PWM methods, and provides guidance for simple practical implementation which is favorable over the conventional methods (space vector or scalar). The experimental results verify the feasibility of the proposed approach.

2. Generalized Scalar PWM Pproach

The generalized scalar PWM approach provides degrees of freedom in the choice of both the zero-sequence signal and the carrier waves. First, the zero-sequence signals can be arbitrarily generated, but generating them based on the phase reference voltages (original modulation signals) provides significant advantages. Until present, most useful PWM pulse patterns could be obtained by this approach. Therefore, in most cases, the zero-sequence signals are obtained by evaluating the reference voltages. Second, the carrier waves of different phases can be selected arbitrarily. However, recent studies have illustrated that employing triangular carrier waves at the same frequency, and selecting the phase relation between the carrier waves of different phases based on the voltage references yields favorable results. As a result, the generalized scalar PWM approach will favor such constraints for the purpose of keeping the scope of the paper within practical boundaries further relaxing the constraints and investigating alternative pulse pattern switch favorable characteristics is a subject matter of future research. Given the described set of constraints, the generalized block diagram of scalar PWM approach with zero-sequence signal injection principle is illustrated in Fig. 3.

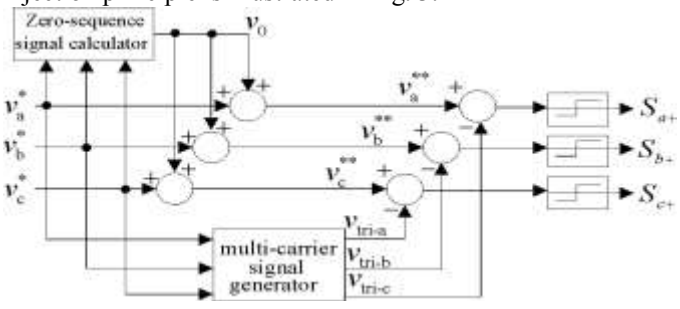

Fig. 3. Block diagram of the generalized carrier-based scalar PWM employing the zero-sequence signal injection principle and multicarrier signals.

. In the generalized scalar approach; according to the original three-phase sinusoidal reference signals (voltage references with single star superscripts) and zero-sequence signals, the final reference (modulation) signals (voltage references with double star superscripts) are generated.

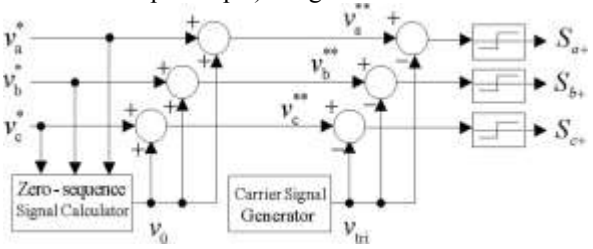

Fig. 4. Block diagram of the conventional scalar PWM method employing zero-sequence signal injection and a common triangular carrier wave.

Then, the individual modulation and carrier waves are compared to determine the associated inverter leg switch states and output voltages. In the conventional approach (see Fig. 6), which is the special case of generalized approach; only one triangular carrier wave is utilized for all phases. In the scalar representation, the modulation waves are defined as follows:

$$V_a{**} = V_a{*} + V_0 = V_{1m} * \cos(\omega_e t) + V_0 \quad (1)$$

$$V_b{**} = V_b{*} + V_0 = V_{1m} * \cos(\omega_e t - 2\pi/3) + v0 \quad (2)$$

$$V_c{**} = V_c{*} + V_0 = V_{1m} * \cos(\omega_e t + 2\pi/3) + v0 \quad (3)$$

Where V_a,, V_b and V_c are the original sinusoidal reference signals and V_0 is the zero-sequence signal. Using the zero-sequence signal injected modulation waves, the duty cycle of each switch can be easily calculated in the following for both single and multicarrier methods:

$$dx+ = (1/2)(1 + v_x{**}/(V_{dc}/2)), \text{ for } x * \{a, b, c\} \quad (4)$$

$$dx- = 1 - dx+, \text{ for } x * \{a, b, c\}. \quad (5)$$

It is helpful to define a modulation index (*Mi*, voltage utilization level) term at this stage. voltage ($V1m$-6-step = $2Vdc/\pi$) is termed the modulation index *Mi* [1]

For a given dc-link voltage (Vdc), the ratio of the fundamental component magnitude of the line to neutral inverter output voltage ($V1m$) to the fundamental component magnitude of the six-step mode

$$Mi = V1m/V1m\text{-6-step} \quad (6)$$

There are two commonly used zero-sequence signals in practical applications. The zero-sequence signal of the widely utilized continuous PWM (CPWM) methods is generated by employing the minimum magnitude test which compares the magnitudes of the three phase original reference signals and selects the signal which has minimum magnitude. Scaling this signal by 0.5, the zero sequence signal of these CPWM methods is found. Assume $|v*a| \le |v*b|, |v*c|$, then $v0 = 5 \cdot v*a$. This modulation wave is recognized as SVPWM

modulation wave in [1]. Inside the voltage linearity region, in the CPWM methods, the modulation waves are always within the carrier triangle peak boundaries; within every carrier cycle, the triangle and modulation waves intersect, and ON and OFF switching always occur. In discontinuous PWM (DPWM) methods, the zero-sequence signal is injected such that reference signal of one phase is always clamped to the positive or negative dc bus. The clamped phase is alternated throughout the fundamental cycle. In the most common DPWM modulation wave (in the literature recognized as the DPWM1 modulation wave), the phase signal which is the largest in magnitude is clamped to the dc bus with the same polarity [1]. Assume $|v^*a| \geq |v^*b|, |v^*c|$, then $v0 = (\text{sign}(v^*a)) \cdot (Vdc/2) - v^*a$. The inverter leg whose modulation wave is clamped to the dc bus is not switched; therefore, switching losses are reduced in DPWM methods. Using the discussed CPWM modulation wave along with a common triangular carrier wave for all phases, SVPWM method yields. Likewise, using the discussed DPWM modulation wave along with a common triangular carrier wave for all phases, DPWM1 yields. Using the same modulation waves, but varying the triangle polarities (resulting in multicarrier waves, $v$tri-a , $v$tri-b , $v$tri-c) additional methods yield... Thus, the proposed approach is broad and covers most methods reported in the literature. Considering that the methods reported in this paper (both conventional and the recently developed RCMV–PWM methods) and the other conventional methods are the most popular methods (due to their superior performance when compared to other methods), the approach yields sufficient results from the practical utilization perspective. Using the proposed approach and creating a variety of triangular carrier wave patterns and modulation wave shapes, further PWM pulse patterns, and thus new methods can be invented. This paper will be confined to the methods discussed in this paragraph. However, it can be shown that they can be included under the generalized scalar PWM umbrella. In the alternating polarity triangular carrier wave methods, the alternating triangle polarities, for example those in Table I, can be obtained by determining the regions of Fig. 4. This goal can be easily achieved by comparing the modulation waves. For example, the $v^*a \geq v^*b, v^*c$ condition corresponds to the A1 region. Such operations can be very easily performed with the PWM units of the modern digital signal processors used in ac motor drives and PWM rectifiers. Before getting involved in implementation details and experimental results, the aforementioned discussed PWM methods will be reviewed in terms of pulse patterns and performance.

3. Pulse Patterns and Performance Characteristics of Popular PWM Methods

Since a large number of PWM methods exist and each method with unique pulse pattern yields unique performance characteristics, full investigation of all PWM methods in regard to their pulse pattern and performance is a laborious task. However, the theoretically infinite choice of methods, in practice reduces to a relatively small count when a systematic evaluation and performance comparison (among the many methods) is made. This section aims to review the popular PWM methods with the focus on their pulse patterns such that in the following section the practical implementation can be discussed to sufficient depth. Observing the pulse patterns, the performance characteristics can be studied, and thus major advantages of these methods can be recognized. Therefore, while reviewing the pulse patterns of the popular methods, it will also be possible to demonstrate why these methods are so well accepted. The pulse pattern of SVPWM is illustrated in Fig. 8 for the region A1. With equally partitioned two zero states [(0 0 0) and (1 1 1)], SVPWM provides very low PWM ripple and provides voltage linearity for the modulation index range of $0<Mi<0.907$. As it has symmetric zero stages, from the PWM ripple reduction perspective SVPWM is the best method. But as Mi increases the ripple also increases and it loses its advantage around $Mi \approx 0.6$ where discontinuous PWM methods can be used .For example increasing the switching frequency by 50% and employing the DPWM1 method for region A1∩B2 the switching count and, therefore, the switching losses remain the same (as one of the phases ceases switching during the PWM period) while the ripple of DPWM1 becomes less compared to SVPWM. Due to reduction of the total zero state duty cycles at high Mi and 50% increase of the carrier frequency (decrease of the carrier cycle), the effect of the zero states on ripple decreases and they can be lumped.Thus, low ripple or low loss results. Consequently, SVPWM at lowMi , and DPWM1 at high Mi have been widely used. It has been illustrated that transition between methods is seamless (the load current is not disturbed) and a combination of the two methods has been successfully used in commercial drives.

However, for both SVPWM and DPWM1, as shown at the bottom of the pulse pattern diagrams, the inverter CMV is high. In motor drive applications, higher CMV is associated with increased common mode current (motor leakage current), higher risk of nuisance trips, and reduced bearing life.The CMV of the three-phase VSI is defined as the potential of load star point with respect to the midpoint of dc bus of the inverter and the CMV at the inverter output can be expressed as follows:

$$vcm = (vao + vbo + vco)/3 . \quad (7)$$

the CMV of SPWM, SVPWM, and DPWM1 methods (and all other common carrier wave PWM methods), may take the values of $V_{dc}/6$ or $V_{dc}/2$; depending on the inverter switch states. As these methods utilize zero vectors V_0 and V_7, a CMV of $-V_{dc}/2$ and $V_{dc}/2$ can be created. This high CMV is illustrated in Figs. 8 and 9(a) at the bottom traces. Since they do not utilize zero states, NSPWM, AZSPWM1, and AZSPWM3 (and all other RCMV PWM methods) avoid a CMV with a magnitude of $V_{dc}/2$ and their CMV magnitude is confined to $V_{dc}/6$. Comparing the pulse patterns of Fig. 9(a) and (b), it can be observed that NSPWM is a discontinuous

PWM method and it yields equivalent advantages to DPWM1 in terms of switching loss reduction. This is obtained differently from the DPWM1 method.

While in DPWM1 one of the zero states is avoided, in NSPWM both zero states are avoided and an active vector is introduced instead. The switching count reduction is obtained by proper sequencing the voltage vectors. Similar to DPWM1, its ripple is low in the high M_i range as the active vectors close to the reference voltage vector dominate.The main disadvantage of NSPWM involves voltage linearity. NSPWM is only linear in the range of $0.61 \leq M_i \leq 0.907$ (DPWM1 linearity range: $0 < M_i < 0.907$). While in PWM rectifier applications this range is sufficient, in motor drives operation at low M_i is required and NSPWM must be combined with another method. In motor drive applications, operating at lowM_i and obtaining low CMV is possible by employing AZSPWM1 or AZSPWM3 in this range. The two AZSPWM methods yield low CMV with $V_{dc}/6$ magnitude and AZSPWM3 has a lower CMV frequency which is favorable. However, it has simultaneous switching actions which may yield undesirable results of motor terminal overvoltage or increased leakage current during switching instants (similar to RSPWM and AZSPWM2). As a result, while AZSPWM1 has found application AZSPWM3 has been cautiously approached. It should also be noted that AZSPWM methods have very high ripple at low M_i (due to the fact that the zero states are replaced with active vectors with opposite direction to the reference voltage vector) and at high M_i they are inferior to NSPWM as the switching losses are higher [16]. Thus, although they are linear in the range of $0 < M_i < 0.907$, AZSPWM methods should only be used in regions where all other methods do not meet the performance requirements of an inverter drive. It should be noted that in all PWM methods, the injected zero sequence signal is a low-frequency signal (periodic at $3\omega_e$ and/or its multiples, lower than the carrier frequency by at least an order of magnitude) which causes low-frequency CMV. At such frequencies the parasitic circuit components (capacitances) are negligible (open-circuit) and, therefore, the zero-sequence voltage has no detrimental effect on the drive and yields no common mode current (CMC), unless low common mode impedance path is provided by filter configurations included in the drive for the purpose of ripple reduction . High-frequency CMV, on the other hand, can be harmful and can be reduced by PWM pulse pattern modification. Thus, the high-frequency CMV effects (at the carrier frequency and higher) have been considered here.

Fig 5: Pulse pattern

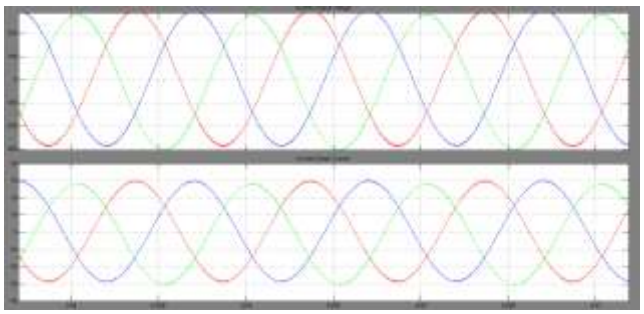

Fig 6: voltage and current waveforms

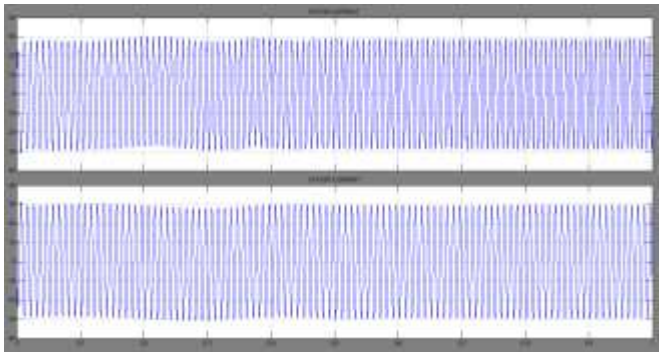

Fig 7: Rotor Current and Stator Current

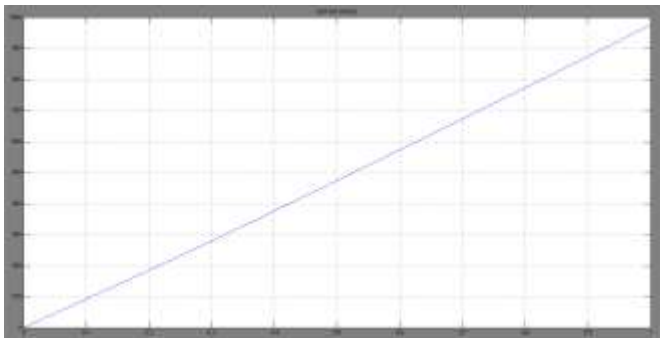

Fig 8: Rotor Speed

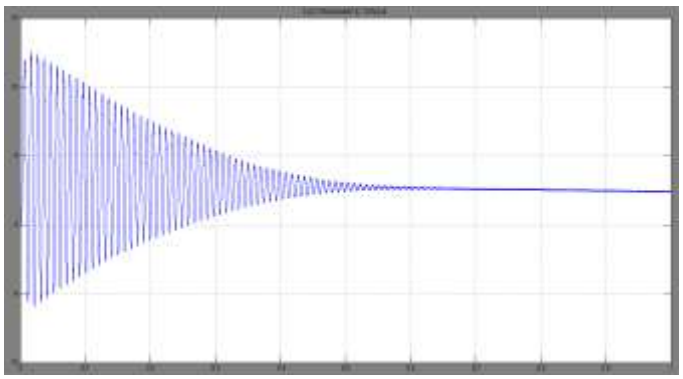

Fig 9: Electromagnetic Torque

4. Implementation

In this section, the practical implementation of the PWM methods of Section IV is discussed. Only several comparisons among the three sinusoidal references (original modulation waves) and several algebraic operations are necessary to obtain the zero-sequence signal, as shown in Section III via examples. Having obtained the zero sequence signal, it is added to the original modulation waves and the final modulation signals result. The duty cycles are checked and bounded to the range of 0 to 1 (in case over modulation condition occurs). For SVPWM and DPWM1, a common triangular carrier wave and for AZSPWM1, AZSPWM3, and NSPWM using a common triangular carrier wave but alternating its polarity according to Table I, are generated. Determining the triangle polarity also involves only a comparison of the sinusoidal references. These operations can be lumped together with the zero-sequence signal determination stage to further minimize the computational burden. This task is left to the implementation engineer as a straightforward procedure. Once the final modulation signals and triangles are obtained, the remaining task involves the sine-triangle comparison stage. This comparison is performed to determine the switching instants via a comparator for each phase. The scalar PWM implementation of all the discussed methods is an easy task compared to the space vector implementation (discussed at the end of Section II). The implementation can be best realized on digital PWM units such as the modern motion control or power management microcontrollers and DSP chips (which involve a well developed software programmable digital PWM unit). Most modern commercial drives and power converters utilize such control chips which are offered at economical price. Thus, the approach can be readily employed in most power converter control platforms. Employing such digital platforms, and considering the simplicity of the scalar PWM algorithms, it is easy to program (combine) two or more PWM methods and online select a modulator in each operating region in order to obtain the highest performance [1]. Combination of SVPWM at low M_i and DPWM1 at high M_i is common in industrial drives. Combination of AZSPWM methods at low M_i and NSPWM at high M_i is an alternative approach for low CMV requiring applications While operating at high M_i (such as full speed operation of a drive or PWM rectifier operating under the normal operating range), over modulation condition may occur due to dynamics or other line or load variation conditions.

5. Experimental Results

In the laboratory, the discussed PWM methods are implemented using the Texas Instruments TMS320F2808 fixed-point DSP chip. In this chip, the PWM signals are generated by the enhanced PWM (EPWM) module of the DSP [30] which is a hardware digital circuit dedicated for the purpose of generating the PWM signals. The PWM period (thus the switching frequency), the dead time, etc. are all parameters that are controlled by the user via software. The EPWM module includes an internal counter clock (termed as "PERIOD") which corresponds to the triangular carrier wave. The value of this counter defines the half of the PWM period. One carrier cycle is completed as the counter counts up from "0" to "PERIOD" and then decrements down to "0" again. For every PWM cycle, the per phase duty cycles are calculated first. Then, the duty cycles are converted to the count number as they are scaled with the PERIOD. Since the EPWM module has two comparator registers (COMPA and COMPB) per phase, the count number, its complementary, zero (0), or PERIOD value are loaded to these counters depending on the pulse pattern to be generated. In this application, the switching rule is defined as the PWM signal of the upper switch of an inverter phase (for instance, S_{a+}) is at logic level "1" when the counter value is between the loaded values of comparator register A (COMPA) and comparator register B (COMPB) comparator registers and at logic "0" otherwise (S_{a-} logic is complementary of S_{a+}).The conventional PWM pulse patterns are generated such that the PWM cycle starts and ends with the upper switches in the high "1" state, (often termed as "active high" except for the PWM periods where the switching ceases in DPWM methods.. Employing the scalar implementation approach and utilizing the TMS320F2808 DSP platform, PWM signals are programmed and applied to a three-phase VSI. This demonstrates that all the intended pulse patterns can be easily generated. Note that SVPWM utilizes zero vectors (000) and (111) which cause a CMV of $-V_{dc}/2$ and $V_{dc}/2$, respectively. In AZSPWM1, only active switch states are utilized; thus, the CMV is limited to $V_{dc}/6$. While in SVPWM the line-toline voltages are unipolar, AZSPWM1 line-to-line voltages are bipolar. Bipolar voltage pulses result in higher output current ripple compared to unipolar voltage pulses, and they may cause overvoltages at the motor terminals in long-cable applications. A 4 kW, 1440 min^{-1} , 380 V_{ll-rms} induction motor is driven from the VSI in the constant *V/f* mode (176.7 V_{rms}/50 Hz) and the PWM frequency is 6.6 kHz for CPWM methods and 10 kHz for DPWM methods to provide equal average switching frequency. Operation at M_i = 0.8 (180.3 V_{rms}/51 Hz, 1510 min^{-1}) is discussed. As can be seen from the diagrams all the discussed methods provide satisfactory performance at the high M_i . NSPWM provides low motor current ripple and CMV/CMC. SVPWM and DPWM1 have low current ripple but high CMV/ CMC. AZSPWM3 has high CMV and CMC magnitude compared to NSPWM, but its CMV/CMC frequency is less. AZSPWM1 has higher PWM current ripple and comparable CMV/CMC to NSPWM. The aforementioned waveforms demonstrate that the various PWM methods can be easily implemented with the generalized scalar PWM approach.

6. Conclusion

PWM principles are reviewed for three-phase, three-wire inverter drives. The characteristics, pulse patterns, and implementation of the popular PWM methods are discussed.

The generalized scalar PWM approach is established and it is shown that it unites the conventional PWM methods and most recently developed reduced common mode voltage PWM methods under one umbrella. Through a detailed example, the method to generate the pulse patterns of these PWM methods via the generalized scalar PWM approach is illustrated. It is shown that the generalized scalar approach yields a simple and powerful implementation with modern control chips which have digital PWM units. With this approach, it becomes an easy task to program the pulse patterns of various high performance PWM methods and benefit from their performance in modern VSIs for applications such as motor drives, PWM rectifiers, and active filters. The theory is verified by laboratory experiments. It is demonstrated that with the proposed approach both the conventional PWM pulse patterns (such as those of SVPWM and DPWM1) and the recently developed improved high-frequency common mode voltage/current performance method pulse patterns (NSPWM, AZSPWM1, and AZSPWM3) can be easily generated. Applying such pulse patterns to motor drives, it has been demonstrated that NSPWM, AZSPWM1, and AZSPWM3 methods provide good performance. Thus, the inverter design engineers are encouraged to include such pulse patterns in their designs.

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The authors have no conflicts of interest to declare that are relevant to the content of this article.