On a Quasi Optimal Algorithm for Analog Circuits Optimization

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Abstract: - An analog circuit design methodology based on applications of control theory is the basis for constructing an optimal or quasi-optimal design algorithm. The main criterion for identifying the required structure of the algorithm is the behavior of the Lyapunov function, which was decisive for the circuit optimization process. The characteristics of the Lyapunov function and its derivative are the basis for finding the optimal structure of the control vector that determines the structure of the algorithm. A block diagram of a quasi-optimal algorithm that implements the main ideas of the methodology is constructed, and the main characteristics of this algorithm are presented in comparison with the traditional approach.

Key-Words: - Circuit design, time-optimal algorithm, control theory, Lyapunov function, control vector structure, quasi optimal algorithm.

Received: November 7, 2020. Revised: May 16, 2021. Accepted: May 20, 2021. Published: June 12, 2021.

1 Introduction

The computer time reduction of a large system design is one of the sources of the total quality design improvement. This problem has a great significance because it has a lot of applications, for example on VLSI electronic circuit design. Any traditional system design strategy includes two main parts: the mathematical model of the physical system that can be defined by the algebraic equations or differential-integral equations and optimization procedure that achieves the optimum point of objective function of designing. In limits of this conception it is possible to change optimization strategy and use the different models and different methods of analysis but in each step of the circuit optimization process there are a fixed number of the equations of the mathematical model and a fixed number of the independent parameters of the optimization procedure.

There are some powerful methods that reduce the necessary time for the circuit analysis. Because a matrix of the large-scale circuit is a very sparse, the special sparse matrix techniques are used successfully for this purpose [1-2]. Other approach to reduce the amount of computational required for both linear and nonlinear equations is based on the decomposition techniques. The partitioning of the circuit matrix into bordered-block diagonal form can be done by branches tearing as in [3], or by nodes tearing as in [4] and jointly with direct solution algorithms gives the solution of the problem.

The extension of the direct solution methods can be obtained by hierarchical decomposition and macromodel representation [5]. Other approach for achieving decomposition at the nonlinear level consists on a special iteration techniques and has been realized in [6] for the iterated timing analysis and circuit simulation. Optimization technique that is used for the circuit optimization and design, exert a very strong influence on the total necessary computer time too. The numerical methods are developed both for the unconstrained and for the constrained optimization [6] and will be improved later on.

Different techniques for analog circuit optimization can be classified in two main groups: deterministic optimization algorithms and stochastic search algorithms. Some drawbacks of classic deterministic optimization algorithms consist in requirement of a good initial point in space of parameters, unsatisfactory local minimum that can be reached, and very often in requirement of continuity and differentiability of the objective function. To overcome these problems some special methods were applied. For example a method to

determine initial point of the process by centering [7], application of geometric programming methods [8] that guarantee the convergence to a global minimum, but, on the other hand, this require a special formulation of design equation to which additional difficulties accompany. Other approach based on the idea of space mapping technique [9]. The aim of space-mapping is to achieve a satisfactory solution with a minimal number of computationally expensive fine model evaluations by means of optimization of coarse model. This technology successfully used for optimization of microwave systems but there are no experience for solution other problems.

Stochastic search algorithms, especially evolutionary computation algorithms like genetic algorithms, differential evaluation, genetic programming, particle swarm optimization, etc. have been developed in recent years [10-15]. Genetic algorithms have been employed as optimization routines for analog circuits due to the ability to find a satisfactory solution. A special algorithm defined as a particle swarm optimization technique is one of the evolutionary algorithms and competes with genetic algorithms. This method is successfully used for electromagnetic problems and for optimization of microwave systems [16-17].

The practical aspects of deterministic methods were developed for the electronic circuits design with the different optimization criterions [18]. The fundamental problems of the development, structure elaboration, and adaptation of the automation design systems have been examine in some papers [19-20].

The above described ideas of system design as deterministic and stochastic can be named as the traditional approach or the traditional strategy because the analysis method is based on the Kirchhoff laws.

The idea of refusing of laws of Kirchhoff at designing of electronic circuits was outspoken in [21] and realized practically in two systems of designing [22-23]. The most general approach was realized at development of the generalized methodology of process of optimization of electronic circuit, defined as the controllable dynamic system [24]. This system is determined by differential or numerical equations for state variables and a system of constraints which is defined by the mathematical model of electronic circuit. The main conception of this theory is the introduction of the special control vector, which generalizes the network optimization process and gives the possibility to control the design process to achieve an optimum of the cost function of the designing for the minimal computer time. This possibility appears due to an infinite number of the different strategies of designing that exist within this theory. By this approach the traditional strategy of designing is only a one representative of a large set of different designing strategies. As shown [24] the potential computer time gain that can be obtained by this approach is increased when the size and complexity of the system increase.

2 Problem Formulation

We will consider that the process of designing of electronic circuit is formulated as a task of minimization of not negative special objective function $C(X)$. It is assumed that all aims of designing are realized it in the point of a minimum of objective function $C(X)$.

In case of differential form for optimization procedure the system of equations for state variables can be written in procedure of optimization [24] by this form:

$$\frac{dx_i}{dt} = f_i(X,U), \quad i = 1,2,...,N, \tag{1}$$

where N is an incurrence of variables in the task of optimization of electronic circuit, $U = (u_1, u_2, ..., u_M)$ is a vector of control functions, $u_j \in \Omega$, $\Omega = \{0;1\}$. According to the developed methodology, the system of constraints of the procedure of optimization, being at sense the mathematical model of electronic circuit, can be defined by means of the next equations:

$$(1 - u_j) g_j(X) = 0, \quad j = 1,2,..., M, \tag{2}$$

where M is a number of dependency variables, coincide with the number of nods of circuit.

Functions $f_i(X,U)$ can be determined by one or another method of optimization and, in particular, for the gradient method of optimization, the functions $f_i(X,U)$ are given as follows [24]:

$$f_i(X,U) = -\frac{\delta}{\delta x_i} F(X,U), \qquad i = 1,2,...,K, \tag{3}$$

$$f_i(X,U) = -u_{i-K} \frac{\delta}{\delta x_i} F(X,U) + \frac{(1-u_{i-K})}{dt}\left[-x_i^{'} + \eta_i(X)\right],$$
$$i = K+1, K+2, ..., N, \tag{3´}$$

where K is a number of independent variables in the traditional definition of task (N=K+M), function

$\eta_i(X)$, written in implicit form and it defines a current value of variable x_i from the system (2), $x_i^{'}$ is a previous variable value x_i. A function $F(X,U)$ is the generalized objective function of designing process and can be defined by the next additive expression [24]:

$$F(X,U) = C(X) + \frac{1}{\varepsilon}\sum_{j=1}^{M} u_j g_j^2(X). \quad (4)$$

It is necessary to find the optimal behavior of the control functions u_j during the design process to minimize the total design computer time. The functions $f_i(X,U)$ are piecewise continued as the temporal functions and the structure of these functions can be found by approximate methods of the control theory [25-26].

In such definition the task of optimization of circuit is formulated as a controllable dynamic system, which needs to bring to a point of equilibrium. Thus the time of transient for the system is associated with the time of designing of electronic circuit. In this case a basic instrument is a control vector of *U* which changes the internal structure of the equations for circuit optimization problem.

3 Lyapunov Function

Dynamic properties of designing process were analyzed [27] on the basis of the entered function of Lyapunov of process of optimization. The presence of the correlation was marked between processor time of optimization of circuit and properties of function of Lyapunov of process of optimization. It was showed that the function of Lyapunov can be defined on the basis of the generalized objective function of process of optimization $F(X,U)$ by means of the next formula:

$$V(X,U) = [F(X,U)]^r, \quad (5)$$

where degree of $r > 0$.

We can define now the design process as a transition process for controllable dynamic system that can provide the stationary point (final point of the optimization procedure) during some time. The problem of the time-optimal design algorithm construction can be formulated now as the problem of the transition process searching with the minimal transition time. There is a well-known idea [28-29] to minimize the time of the transition process by means of the special choice of the right hand part of the principal system of equations; in our case these are the functions $f_i(X,U)$. It is necessary to change the functions $f_i(X,U)$ by means of the control vector *U* selection to obtain a maximum speed of the Lyapunov function decreasing (maximum absolute value of the Lyapunov function time derivative $\dot{V} = dV/dt$).

The problem of stability of designing trajectory is related to the analysis of conduct of derivative at times from the function of Lyapunov $\dot{V}$. More informative however there is the normalized derivative on time, which is defined by next formula:

$$W = \dot{V}/V. \quad (6)$$

In this case we can compare the different design strategies by means of the function *W(t)* behavior and we can search the optimal position for the control vector switch points.

It was showed [30] that on the basis of analysis of conduct of derivative function of Lyapunov it is possible to find optimum switch points of control vector *U* that is a basis of quasi optimal strategy of designing and allowing to minimizing processor time of designing.

4 Optimal Switch Point

The optimal structure of the control vector *U* is the principal aim of the analysis of process of designing that is based on generalized methodology. All examples were analyzed for the continuous form of the optimization procedure (1). Functions *V(t)* and *W(t)* were the main objects of the analysis and its behavior has been analyzed during the design process. As shown in [30] the behavior of the functions *V(t)* and *W(t)* can define the total computer time for each design strategy. It is very interesting to analyze the behavior of the function *V(t)* for determine the optimal position of the switch points of the control vector. This function serves as a sensitive criterion to detect the optimal switching of the control vector *U*. The Lyapunov function *V(t)* for all examples was calculated by formula (5) for $r = 0.5$.

4.1 Example 1

The analysis of the process of designing for two-node passive nonlinear network in Fig. 1 is presented below.

The model of this network (2) includes two equations (M=2) and the optimization procedure (1) includes five equations.

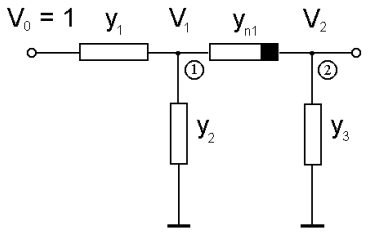

Fig. 1 Two-node nonlinear passive network

The nonlinear element is defined as: $y_{n1} = a_{n1} + b_{n1} \cdot (V_1 - V_2)^2$. The vector X includes five components: $x_1^2 = y_1$, $x_2^2 = y_2$, $x_3^2 = y_3$, $x_4 = V_1$, $x_5 = V_2$. This network is characterized by two dependent parameters and the control vector includes two control functions: $U = (u_1, u_2)$. Structural basis includes four different strategies with corresponding control vector: (00), (01), (10), and (11). Behavior of the functions *V(t)* and *W(t)* help us to determine the switch point optimal position of the control vector.

Taking into account the preliminary reasons about the optimal algorithm structure [24] we have been analyzed the strategy that consists of two parts. The first part is defined by the control vector (11) that corresponds to MTDS and the second part is defined by the control vector (00) that corresponds to TDS. So, the switching is realized between two strategies, (11) and (00).

The behavior of the functions *V(t)* and *W(t)* during the process of circuit design after the switching point is shown in Fig. 2.

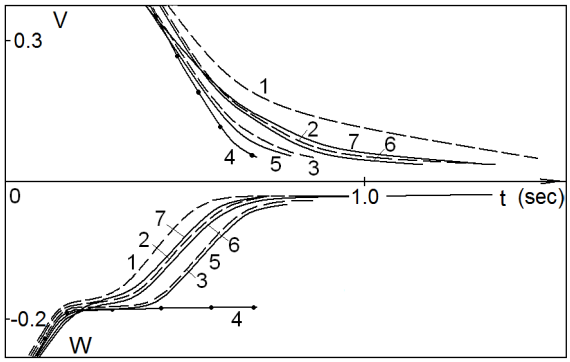

Fig. 2 Behavior of the functions *V(t)* and *W(t)* in the design process for seven different switch points (from 147 to 267)

The corresponding total iteration number and computer time are presented in Table 1.

The integration of the system (1) was realized by the constant integration step. The step for switch point increment is equal 20 to improve the identification of the difference between all curves.

Table 1. Iterations number and computer time for strategies with different switch points

N	Switch point	Iterations number	Total design time (sec)
1	147	8319	0.221
2	167	6501	0.172
3	187	3697	0.096
4	207	2860	0.073
5	227	3383	0.087
6	247	5429	0.142
7	267	6682	0.175

The analysis shows that the optimal switch point corresponds to the step 207 (graph 4 with dots in Fig. 2). The curves 1, 2, and 3 correspond to the switch point position before the optimal switch point (curve 4), but the curves 5, 6, and 7 correspond to the switch point that lies after the optimal one. There is a decreasing of the computer time from curve 1 to curve 4. On the contrary, the computer time increases from curve 4 to curve 7. It means that curve 4 corresponds to the optimal position of the switch point.

The initial parts of *W(t)* dependencies of Fig. 2 are shown in Fig. 3 in large scale.

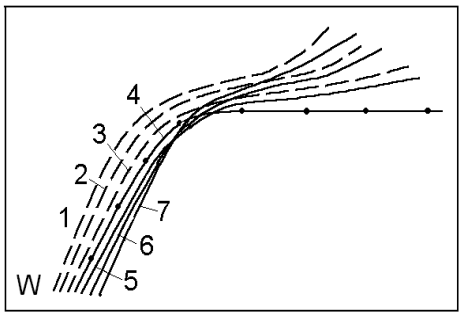

Fig. 3 Behavior of the functions *V(t)* and *W(t)* during the initial part of design process

We can see that the curves 1, 2, and 3, which correspond to the switch points before the optimal point (4) have not intersections. On the other hand, the curves 5, 6, and 7 that are based on the switch point after the optimal one have intersections and each this curve lies upper the curve 4 till some time point. It means that from this time moment the graph *W(t)* for the optimal switch point lies below all of other graph. So, from one hand the optimal switch point corresponds to a minimal computer time, from the other hand, this point corresponds to the graph of *W(t)* function that lies below all of other graphs. This property serves as a principal criterion for the optimal switch point selection.

The function *W(t)* that corresponds to the optimal switch point has a maximum absolute value leading off the 340th integration step. It means that from this integration step we can confidently predict the optimal switch point position that leads to the minimal computer design time.

4.2 Example 2

Three-node nonlinear circuit is presented below in Fig. 4. The nonlinear elements are defined as: $y_{n1} = a_{n1} + b_{n1} \cdot (V_1 - V_2)^2$, $y_{n2} = a_{n2} + b_{n2} \cdot (V_2 - V_3)^2$. The vector X includes seven components: $x_1^2 = y_1$, $x_2^2 = y_2$, $x_3^2 = y_3$, $x_4^2 = y_4$, $x_5 = V_1$, $x_6 = V_2$, $x_7 = V_3$.

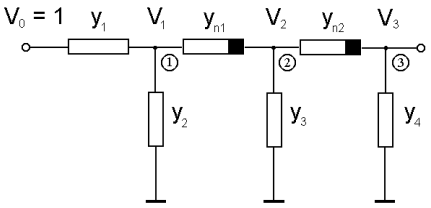

Fig. 4. Three-node nonlinear passive network.

The model of this network (2) includes three equations (*M*=3) and the optimization procedure (1) includes seven equations. This network is characterized by three dependent parameters and the control vector includes three control functions: $U=(u_1, u_2, u_3)$. Structural basis includes eight different strategies with corresponding control vector: (000), (001), (010), (011), (100), (101), (110), and (111). Behavior of the functions *V(t)* and *W(t)* help us to determine the switch point optimal position of the control vector.

Taking into account the preliminary reasons about the optimal algorithm structure [27] we have been analyzed the strategy that consists of two parts. The first part is defined by the control vector (111) that corresponds to Modified Traditional Strategy of Optimization (MTSO) and the second part is defined by the control vector (000) that corresponds to Traditional Strategy of Optimization (TSO). So, the switching is realized between two strategies, (111) and (000).

The optimal switch point was a principal objective of this analysis. The consecutive change of the switch point was realized for the integration step number from 2 to 20. The corresponding total iteration number and computer time are presented in Table 2 for some switch points near the optimal. The behavior of the functions *V(t)* and *W(t)* during the design process after the switch point is shown in Fig. 5 for seven positions of switch points.

Table 2. Iterations number and computer time for strategies with different switch points for three-node network.

N	Switch point	Iterations number	Total design time (sec)
1	6	8409	0.659
2	7	6408	0.502
3	8	3141	0.246
4	9	1234	0.096
5	10	3310	0.259
6	11	5918	0.464
7	12	7404	0.581

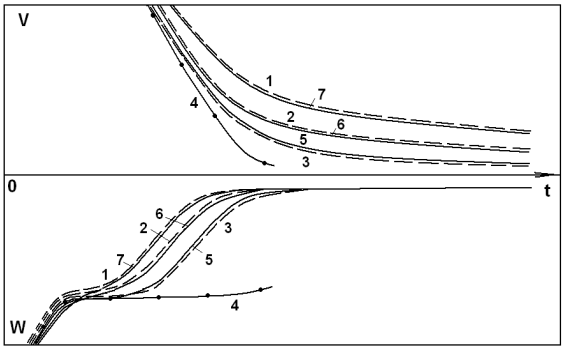

Fig. 5. Behavior of the functions *V(t)* and *W(t)* during the design process for seven different switch points (from 6 to 12) for network in Fig. 4.

The integration of the system (1) was realized by the constant integration step. The analysis shows that the optimal switch point corresponds to the step 9 (graph 4 with dots in Fig. 5). The curves 1, 2, and 3 correspond to the switch point position before the optimal switch point (curve 4), but the curves 5, 6, and 7 correspond to the switch point that lies after the optimal one. There is a decreasing of the computer time from curve 1 to curve 4. On the contrary, the computer time increases from curve 4 to curve 7. It means that curve 4 corresponds to the optimal position of the switch point.

So, from one hand the optimal switch point corresponds to a minimal computer time, from the other hand, this point corresponds to the graph of *W(t)* function that lies below all of other graphs. This property anew serves as a principal criterion for the optimal switch point selection. The function *W(t)* that corresponds to the optimal switch point has a maximum absolute value leading off the 15th integration step. It means that from this integration step we can confidently predict the optimal switch point position that leads to the minimal computer design time.

4.3 Example 3

Five-node nonlinear passive network is shown in Fig. 6.

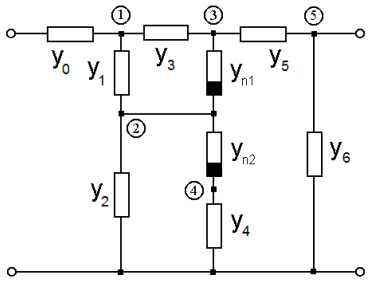

Fig. 6. Five-node nonlinear passive network.

The nonlinear elements have next dependencies: $y_{n1} = a_{n1} + b_{n1} \cdot (V_2 - V_3)^2$, $y_{n2} = a_{n2} + b_{n2} \cdot (V_2 - V_4)^2$. The vector X includes eleven components: $x_1^2 = y_1$, $x_2^2 = y_2$, $x_3^2 = y_3$, $x_4^2 = y_4$, $x_5^2 = y_5$, $x_6^2 = y_6$, $x_7 = V_1$, $x_8 = V_2$, $x_9 = V_3$, $x_{10} = V_4$, $x_{11} = V_5$. The model of this network (2) includes five equations (M=5) and the optimization procedure (1) includes eleven equations. This network is characterized by five dependent parameters and the control vector includes five control functions: $U = (u_1, u_2, u_3, u_4, u_5)$. Structural basis includes 32 different strategies with corresponding control vector from (00000) to (11111). Behavior of the functions *V(t)* and *W(t)* determine the switch point optimal position of the control vector. The switching is realized between strategy (11111) and strategy (00000). The consecutive change of the switch point was realized for the integration step number from 2 to 25.

As discussed above, the principal element of the minimal-time design algorithm is the optimal position of the control vector switch point. The total iteration number and computer time are presented in Table 3 for some switch points near the optimal.

Table 3. Iterations number and computer time for strategies with different switch points for five-node network.

N	Switch point	Iterations number	Total design time (sec)
1	11	62243	28.37
2	12	47371	21.59
3	13	24517	11.17
4	14	1966	0.89
5	15	24163	11.01
6	16	40464	18.44
7	17	49219	22.43

Fig. 7 shows the behavior of the functions *V(t)* and *W(t)* for seven different positions of the switch point.

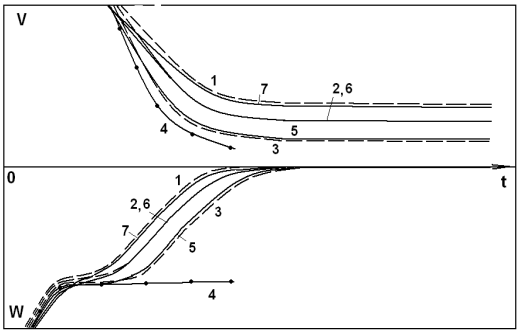

Fig. 7. Behavior of the functions *V(t)* and *W(t)* during the design process for seven different switch points (from 11 to 17) for network in Fig. 6.

It is clear that the optimal switch point corresponds to step 14 and the computer time in this case has a smallest value. The corresponding curve lies below all of the other curves.

4.4 Example 4

The next example corresponds to the two-stage transistor amplifier in Fig. 8.

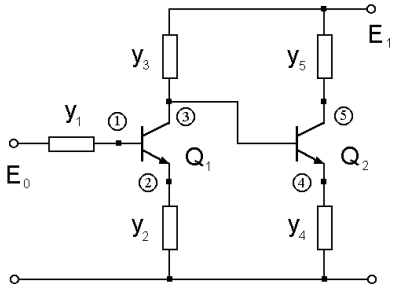

Fig. 8. Two-stage transistor amplifier.

The vector X includes ten components: $x_1^2 = y_1$, $x_2^2 = y_2$, $x_3^2 = y_3$, $x_4^2 = y_4$, $x_5^2 = y_5$, $x_6 = V_1$, $x_7 = V_2$, $x_8 = V_3$, $x_9 = V_4$, $x_{10} = V_5$. The model of this network (2) includes five equations (M=5) and the optimization procedure (1) includes ten equations. The total structural basis contains 32 different design strategies. The control vector includes five control functions: $U = (u_1, u_2, u_3, u_4, u_5)$. The Ebers-Moll static model of the transistor has been used [31].

The total iteration number and computer time for some design strategies are presented in Table 4.

Table 4. Iterations number and computer time for strategies with different switch points for two-stage transistor amplifier.

N	Switch point 1	Switch point 2	Iterations number	Total design time (sec)
1	7	8	4900	9.912
2	8	9	4486	9.113
3	9	10	3785	7.691
4	10	11	1354	2.742
5	11	12	3618	7.341
6	12	13	4424	8.981
7	13	14	4882	9.893

The integration of the system (1) was realized by the optimal variable integration step. Fig. 9 shows the behavior of the functions *V(t)* and *W(t)* for the same design strategies with different switch points including the optimal one.

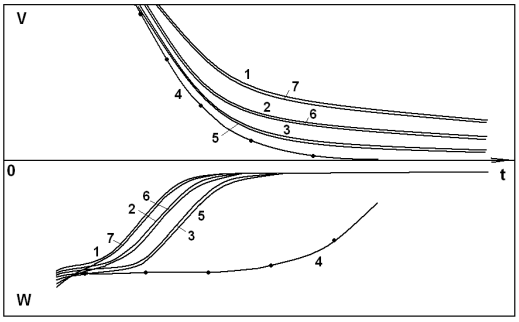

Fig. 9. Behavior of the functions *V(t)* and *W(t)* during the design process for seven different switch points (from 7 to 13) for network in Fig. 8.

As for previous example, the design of two-transistor cell amplifier has been proposed as a combination of MTSO and TSO. In this case the quasi-optimal control vector includes two switch points. We changed the control vector from (11111) to (00000) and from (00000) to (11111). The consecutive change of the switch point was realized for the integration step's number from 2 to 20.The behavior of the functions *V(t)* and *W(t)* for the optimal switch steps and some steps near the optimal confidently detect the optimal position of the switch points.

We observe a specific behavior of the function *W(t)* near the optimal switch point's position. Before the optimal switch point the function *W(t)* graphs are "parallel". Function *W(t)* has the maximum negative value for the optimal switch points. The graphs of the function *W(t)* that correspond to the optimal switch point's position (number 4) and before the optimal position (1, 2 and 3) have not intersection. After the optimal points the graphs of the function *W(t)* intersect the graphs that correspond to the optimal switch point and before the optimal one. It means that we can detect the optimal position of the switch points during the initial design interval.

So, the structure of the optimal control vector i.e. the structure of the time optimal design strategy can be defined by means of the analysis of the relative time derivative of the Lyapunov function during the initial time interval of the design process.

4.5 Example 5

The last example corresponds to the three-stage transistor amplifier in Fig. 10.

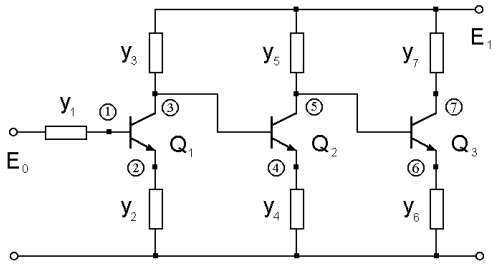

Fig. 10. Three-stage transistor amplifier.

The vector X includes 14 components: $x_1^2=y_1$, $x_2^2=y_2$, $x_3^2=y_3$, $x_4^2=y_4$, $x_5^2=y_5$, $x_6^2=y_6$, $x_7^2=y_7$, $x_8=V_1$, $x_9=V_2$, $x_{10}=V_3$, $x_{11}=V_4$, $x_{12}=V_5$, $x_{13}=V_6$, $x_{14}=V_7$. The model of this network (2) includes seven equations (M=7) and the optimization procedure (1) includes 14 equations. The total structural basis contains 128 different design strategies. The control vector includes seven control functions: $U=(u_1,u_2,u_3,u_4,u_5,u_6,u_7)$.

The total iteration number and computer time are presented in Table 5 for some switch points near the optimal one.

Table 5. Iterations number and computer time for strategies with different switch points for three-stage transistor amplifier.

N	Switch point 1	Switch point 2	Iterations number	Total design time (sec)
1	10	16	8187	154.31
2	11	17	7432	140.04
3	12	18	6125	115.36
4	13	19	2087	39.14
5	14	20	10259	193.33
6	15	21	11610	218.81
7	16	22	12372	233.16

Fig. 11 shows the behavior of the functions *V(t)* and *W(t)* for the same optimization strategies.

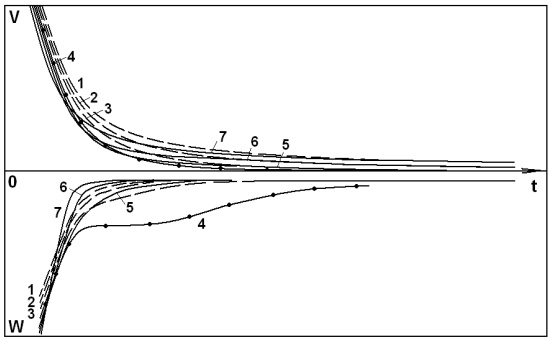

Fig. 11. Behavior of the functions *V(t)* and *W(t)* during the design process for seven different switch points (from 10 to 16) for network in Fig. 10.

The integration of the system (1) was realized by the optimal variable integration step. As for previous example, the design of three-transistor cell amplifier has been proposed as a combination of MTSO and TSO. In this case the quasi-optimal control vector includes two switch points. We changed the control vector from (1111111) to (0000000) and from (0000000) to (1111111). The consecutive change of the switch point was realized for the integration step's number from 2 to 25. The behavior of the functions *V(t)* and *W(t)* for the optimal switch steps and some steps near the optimal confidently detect the optimal position of the switch points. We observe a behavior of the function *W(t)* near the optimal switch point's position similar the previous example. Function *W(t)* has the maximum negative value for the optimal switch points. The graphs of the function *W(t)* that correspond to the optimal switch point's position (number 4) and before the optimal position (1, 2 and 3) have not intersection. After the optimal points the graphs of the function *W(t)* intersect the graphs that correspond to the optimal switch point. It means that we can detect the optimal position of the switch points during the initial design interval.

So, the structure of the optimal control vector i.e. the structure of the time optimal design strategy can be defined by means of the analysis of the relative time derivative of the Lyapunov function for the initial time design interval

We observe a specific behavior of the function *W(t)* near the optimal switch point's position. Before the optimal switch point the function *W(t)* graphs are "parallel". Function *W(t)* has the maximum negative value for the optimal switch points. The graphs of the function *W(t)* that correspond to the optimal switch point's position (number 4) and before the optimal position (1, 2 and 3) have not intersection. After the optimal points the graphs of the function *W(t)* intersect the graphs that correspond to the optimal switch point and before the optimal one. It means that we can detect the optimal position of the switch points during the initial design interval.

5 Quasi Optimal Algorithm

We can mark two special strategies of optimization. The first strategy is determined by a control vector $U = (0,0,...,0)$. This strategy corresponds to the traditional approach for a circuit optimization, and in this case the system (2), being the system of constraints, must be solved on every step of procedure of optimization. This is a traditional strategy of optimization. The second strategy is determined by a control vector $U = (1,1,...,1)$. In this case the system (2) disappears fully, but information about a circuit appears in the generalized objective function (4). This is a modified traditional strategy of optimization. In this case other trajectory corresponds to MTSO in a space of parameters. Flow-charts both TSO and MTSO are represented on Fig. 12 and Fig. 13 correspondingly.

Dynamic properties of designing process were analyzed in [32] on the basis of the entered function of Lyapunov of process of optimization. The presence of the correlation was marked between processor time of optimization of circuit and properties of function of Lyapunov of process of optimization. It was showed that the function of Lyapunov can be defined on the basis of the generalized objective function of process of optimization $F(X,U)$ by means of the formula (5).

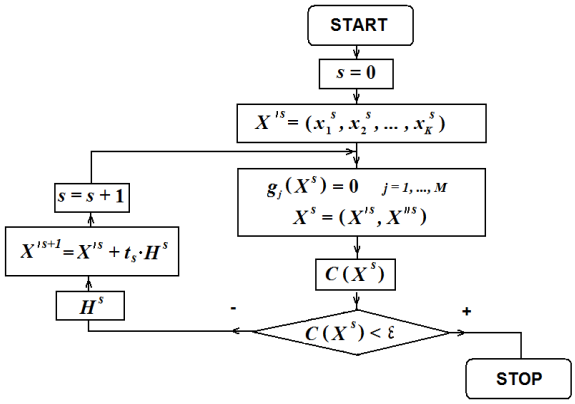

Fig.12. Algorithm of TSO.

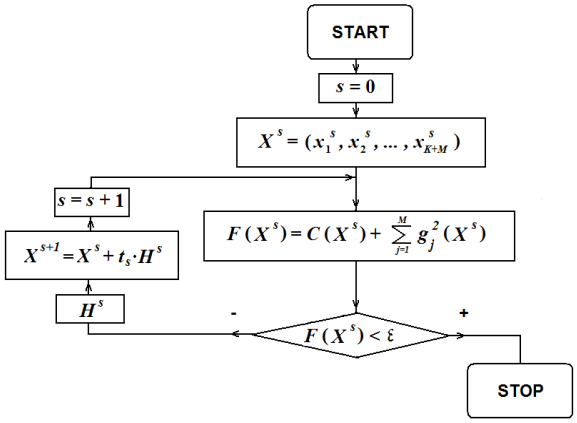

Fig. 13. Algorithm of MTSO.

It was showed [32] that on the basis of analysis of conduct of derivative function of Lyapunov it is possible to find optimum switch points of control vector *U* that is a basis of quasi optimal strategy and allowing to minimizing the CPU time.

We will define elementary structures which serve for the flow-chart construction of quasi optimal algorithm. There are two such structures.

We will define the first structure as a traditional strategy of optimization for one step of optimization procedure (TSO_1). This structure includes:

1. One step of the unconstrained optimization is in space R^K of the independent variables:

$$X'^{s+1} = X'^{s} + t_s \cdot H^s, \qquad (7)$$

where $X' \in R^K$, H is direction of decreasing of objective function $C(X)$, determined one or another method of descent.

2. Solution of the system of nonlinear equations that is the mathematical model of electronic circuit

$$g_j(X) = 0, \quad j = 1,2,\dots,M. \qquad (8)$$

As a result of reproducing of both these steps we get the new values of all co-ordinates of vector *X*.

The second elementary structure is the modified traditional strategy of optimization for one step of optimization procedure ($MTSO_1$) and it includes one step of procedure of unconstrained optimization in space R^N of independent variables

$$X^{s+1} = X^s + t_s \cdot H^s, \qquad (9)$$

where H is direction of decreasing of the generalized objective function $F(X)$. A vector of H is the function of objective function $F(X)$.

On the basis of ideas, presented in [32] and the determinations defined above, one of possible variants of quasi optimal algorithm is developed Clearly, that TSO_1 and $MTSO_1$ will realize the own strategy on one step of the method of optimization. We will consider in future, that these strategies are defined as separate blocks and can be used in call algorithms. The flow chart of quasi optimal algorithm is presented in Fig. 14.

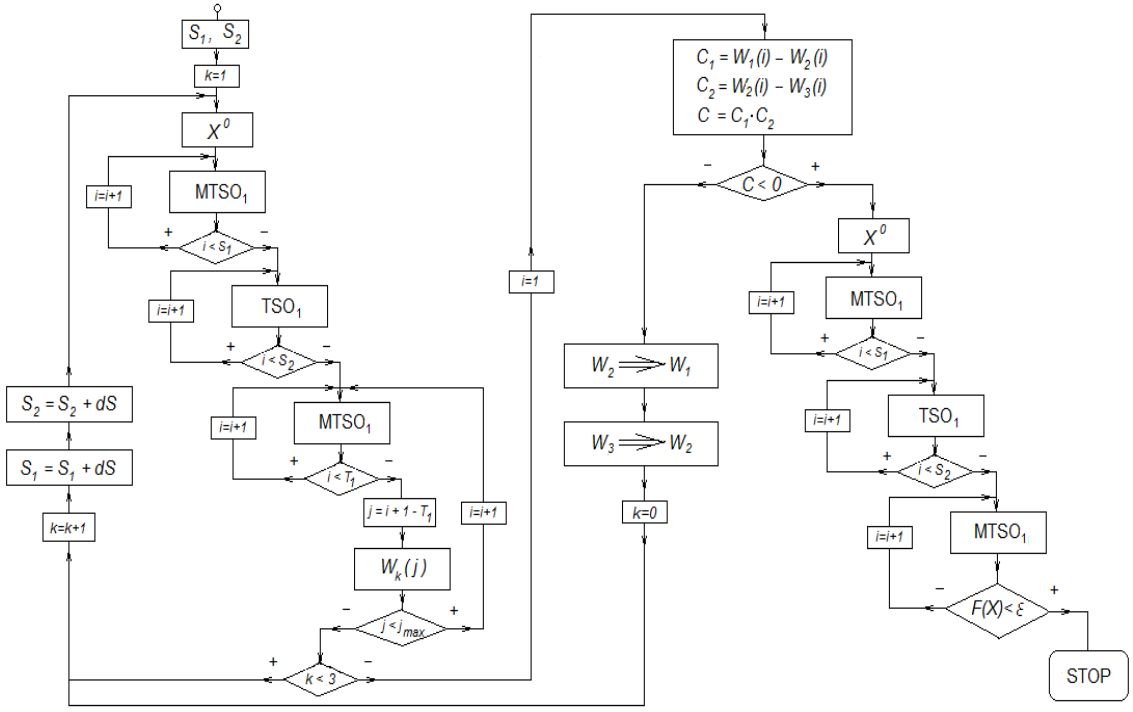

Fig.14. Quasi optimal algorithm

It is assumed that this variant of algorithm is based only on two switching of control vector. Initial switching points of control vector of S_1 and S_2 are set, where for example S_1=1 and S_2=S_1+n. The parameter of n can take on values 1, 2, ... An algorithm begins with MTSO. Then it is switching on TSO in the point of S_1. TSO is executed till switching on MTSO in the point of S_2. MTSO is further executed to the moment of T_1+ j_{max}, where T_1 is set a number in a range 10 – 40, and by a j_{max} number in a range 20 – 80. The values of derivative function of Lyapunov $W_1(t)$ are memorized from the step T_1 till the step T_1+ j_{max}. Then all calculation repeats oneself at the change of switch points on the step dS. The values of relative derivative function of Lyapunov are again memorized, but it already $W_2(t)$. A calculation repeats oneself at a next change on the step of dS and $W_3(t)$ is determined. The analysis of the got results then make and the value of basic criterion of C are produced.

6 Basic Criterion of Principal Algorithm

We will consider the results of analysis of designing process of nonlinear circuit represented on Fig. 15.
At designing of this amplifier, the quasi optimal strategy of designing has a time gain more than 1600 times comparing with traditional approach [33].

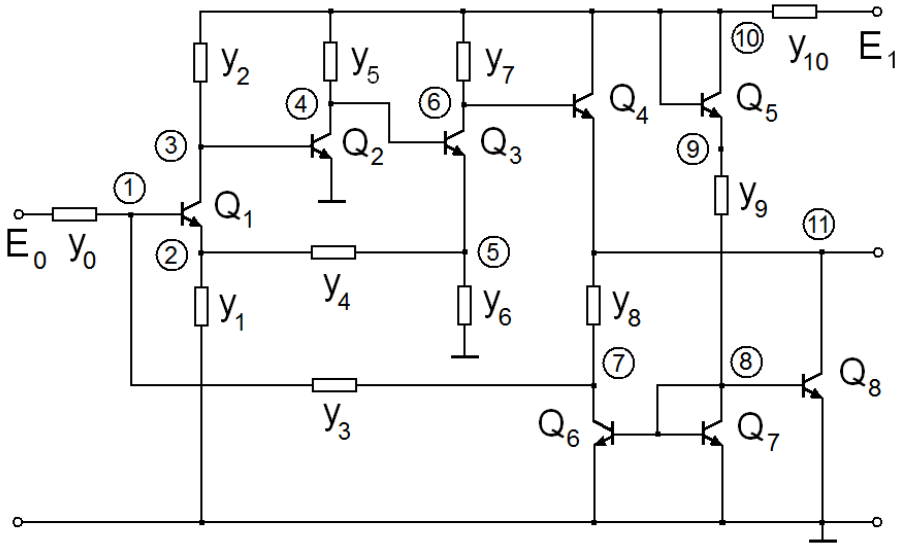

Fig.15. Operational amplifier.

We will consider dependences of functions of $W(t)$ on the initial interval of designing process. These dependences are resulted in Fig. 16.

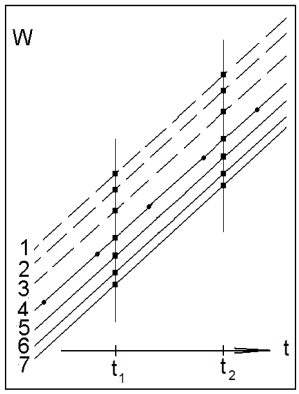

Fig.16. $W(t)$ for some switching points.

The curve 4 corresponds to the optimal point of switching. Three first curves correspond to the points of switching before the optimal point. Three last curves correspond to the points of switching after the optimal point. Distance between the dotted curves is increasing as approaching to the optimum switch point when the corresponding switch point lies before the optimum point. Opposite, a distance between continuous curves, which correspond of switching after an optimum point, is diminished as moving off from an optimum point. It is a good criterion to define an optimum switch point.

We will enter the function of P, determined as a difference of values of function of $W(t)$ for two nearby curves of Fig. 16 in certain moment of time of t. The function P has an argument m, which can be defined as a number of the corresponding curve (1, 2,…), i.e. P is the function of discrete argument.

This function was built for two different values of time of t_1 and t_2, certain on a Fig. 16. Time of t_1 corresponds to 20th step of optimization procedure after a switching point and time of t_2 corresponds to 40th step. The corresponding curves (continuous) are represented in Fig. 17.

This function increases at approaching to the optimum point of switching of control vector. Attaining a maximum the function of P is diminished in further. We will define another function of Q, that is a discrete derivative of the function of P ($Q=P(m+1) -P(m)$) and which is built on the same figure. The conduct of function of Q is such, that it can afford basic for making of basic criterion of quasi optimal algorithm.

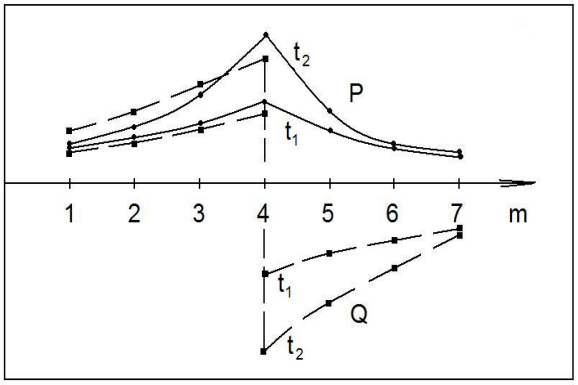

Fig.17. P and Q functions of curve number m.

If we choose as a criterion of C the product of values of function of Q in two nearby points of the argument ($C=Q(m)xQ(m+1)$), a positive value C testifies that an optimum switch point is not yet attained, and the negative value corresponds to an optimum switch point. Thus, calculating the value of functions of P and Q and checking the value of criterion of C into an algorithm, we can exactly define an optimum switch point of control vector. The quasi optimal strategy will be realized after authentication of optimum points of switching. All these details are reflected in an algorithm that presented in Fig. 12.

The developed quasi optimal algorithm give a time gain approximately on 25% less than quasi optimal strategy of designing, that allows to get the real time gain approximately in 1200 times as compared to TSO.

7 Conclusion

The problem of the construction of minimal-time algorithm of designing can be solved adequately on the basis of the control theory. The design process is formulated as the controllable dynamic system. The Lyapunov function of the design process and its time derivative include the sufficient information to select more perspective design strategies from infinite set of the different design strategies that exist into the general design methodology. The special function $W(t)$ was proposed to predict the structure of the time optimal design strategy. This function can be used as a main tool to construct the optimal sequence of the control vector switch points. This is the basis for the optimal design algorithm construction for the system design.

Additional expense of computer time, which related to the search of optimum switch points of control vector, diminishes gain in time that corresponds to the quasi optimal strategy. However, taking into account circumstance that quasi optimal strategy allows getting the general gain in processor time in a few hundred or thousands. A quasi optimal algorithm, i.e. practical realization of quasi optimal strategy, gives the gain of the same order.

References:

[1] J.R. Bunch, and D.J. Rose, (Eds), *Sparse Matrix Computations*, Academic Press, N.Y., 1976.

[2] O. Osterby, and Z. Zlatev, *Direct Methods for Sparse Matrices*, Springer-Verlag, N.Y., 1983.

[3] F.F. Wu, Solution of large-scale networks by tearing, *IEEE Trans. Circuits Syst*., Vol. CAS-23, No. 12, 1976, pp. 706-713.

[4] A. Sangiovanni-Vincentelli, L.K. Chen, and L.O. Chua, An efficient cluster algorithm for tearing large-scale networks, *IEEE Trans. Circuits Syst.*, Vol. CAS-24, No. 12, 1977, pp. 709-717.

[5] N. Rabat, A.E. Ruehli, G.W. Mahoney, and J.J. Coleman, A survey of macro modelling, *Proc. IEEE Int. Symp. Circuits Systems*, 1985, pp. 139-143.

[6] A. George, On Block Elimination for Sparse Linear Systems, *SIAM J. Numer. Anal*. Vol. 11, No.3, 1984, pp. 585-603.

[7] G. Stehr, M. Pronath, F. Schenkel, H. Graeb, and K. Antreich, Initial sizing of analog integrated circuits by centering within topology-given implicit specifications, *Proc. of the IEEE/ACM Int. Conf. CAD*, 2003, pp. 241-246.

[8] M. Hershenson, S. Boyd, and T. Lee, Optimal design of a CMOS op-amp via geometric programming, *IEEE Trans. CAD ICs*, Vol. 20, No. 1, 2001, pp. 1-21.

[9] S. Koziel, J.W. Bandler, and K. Madsen, Space-mapping-based interpolation for engineering optimization, *IEEE Trans. MTT*, Vol. 54, No. 6, 2006, pp. 2410-2421.

[10] D. Nam, Y. Seo, L. Park, C. Park, and B. Kim, Parameter optimization of an on-chip voltage reference circuit using evolutionary programming, *IEEE Trans. Evol. Comput.*, Vol. 5, No. 4, 2001, pp. 414-421.

[11] N.F. Paulino, J. Goes, and A. Steiger-Garcao, Design methodology for optimization of analog building blocks using genetic algorithms, *Proc Symp. CAS*, 2001, pp. 435-438.

[12] G. Alpaydin, S. Balkir, and G. Dundar, An evolutionary approach to automatic synthesis of high performance analog integrated circuits, *IEEE Trans. Evol. Comput.*, Vol. 7, No. 3, 2003, pp. 240-252.

[13] A. Srivastava, T. Kachru, and D. Sylvester, Low-Power-Design Space Exploration Considering Process Variation Using Robust Optimization', *IEEE Trans. CAD ICs*, Vol. 26, No. 1, 2007, pp. 67-79.

[14] B. Liu, Y. Wang, Z. Yu, L. Liu, M. Li, Z. Wang, J. Lu, and F.V. Fernandez, Analog circuit optimization system based on hybrid evolutionary algorithms, *Integr., VLSI Jour.*, Vol. 42, 2009, pp. 137-148.

[15] M.L. Carneiro, P.H.P. de Carvalho, N. Deltimple, L. da C Brito, L.R.A.X. de Menezes, E. Kerherve, S.G. de Araujo, and A.S.Rocira, Doherty amplifier optimization using robust genetic algorithm and Unscented Transform, *Proc. Anual IEEE Northeast Workshop CAS*, 2011, pp. 77-80.

[16] J. Robinson, and Y. Rahmat-Samii, Particle swarm optimization in electromagnetic, *IEEE Trans. Anten. Propag.*, Vol. 52, No. 2, 2004, pp. 397-407.

[17] M.A. Zaman, M. Gaffar, M.M. Alam, S.A. Mamun, and M. Abdul Matin, Synthesis of antenna arrays using artificial bee colony optimization algorithm, *Int. J Microw. Opt. Techn.*, Vol. 6, No. 8, 2011, pp. 234-241.

[18] R.E. Massara, *Optimization Methods in Electronic Circuit Design*, Longman Scientific & Technical, Harlow, 1991.

[19] R.K. Brayton, G.D. Hachtel and A.L. Sangiovanni-Vincentelli, A survey of optimization techniques for integrated-circuit design, *Proc. IEEE*, Vol. 69, 1981, pp. 1334-1362.

[20] A.E. Ruehli, A. Sangiovanni-Vincentelli, and G. Rabbat, Time Analysis of Large-Scale Circuits Containing One-Way Macromodels, *IEEE Trans. Circuits Syst.*, Vol. CAS-29, No. 3, 1982, pp. 185-191.

[21] I.S. Kashirskiy, General Optimization Methods, *Izvest. VUZ USSR -Radioelectronica*, Vol. 19, No. 6, 1976, pp. 21-25.

[22] V. Rizzoli, A. Costanzo, and C. Cecchetti, Numerical optimization of broadband nonlinear microwave circuits, *IEEE MTT-S Int. Symp.*, Vol. 1, 1990, pp. 335-338.

[23] E.S. Ochotta, R.A.Rutenbar, and L.R. Carley, Synthesis of high-performance analog circuits in ASTRX/OBLX, *IEEE Trans. on CAD*, Vol. 15, No. 3, 1996, pp. 273-294.

[24] A. Zemliak, Analog circuit optimization on basis of control theory approach, *COMPEL: The Int. J. Computation and Mathematics in Electrical and Electronic Engineering*, vol. 33, no. 6, pp. 2180-2204, 2014.

[25] R. Sepulchre, M. Jankovic, and P.V. Kokotovic, *Constructive Nonlinear Control*, New York: Springer-Verlag, 1997.

[26] R. Pytlak, *Numerical Methods for Optimal Control Problems with State Constraints*, Berlin: Springer-Verlag, 1999.

[27] A. Zemliak, T Markina, Behaviour of Lyapunov´s function for different strategies of circuit optimization, *International Journal of Electronics*, vol. 102, no. 4, pp. 619-634, 2015.

[28] E.A. Barbashin, *Introduction to the Stability Theory*, Nauka, Moscow, 1967.

[29] N. Rouche, P. Habets, and M. Laloy, *Stability Theory by Liapunov's Direct Method*, Springer-Verlag, N.Y, 1977.

[30] A.M. Zemliak, F. Reyes, S. Vergara, Study of different optimization strategies for analogue circuits, COMPEL: The Int. J. Computation and Mathematics in Electrical and Electronic Engineering, vol. 35, no. 3, pp. 927-942, 2016.

[31] G. Massobrio, P. Antognetti, *Semiconductor Device Modeling with SPICE*, Mc. Graw-Hill, Inc., N. Y., 1993.

[32] A.M. Zemliak, Comparative Analysis of the Lyapunov Function for Different Design Strategies of Analogue Circuits Design, *Radioelectronics and Communications Systems*, Vol. 51, No. 5, 2008, pp. 233-238.

[33] A.M. Zemliak, Analysis of the control vector structure in analog networks design, Radioelectronics and Communications Systems, Vol. 52, No. 10, 2009, pp. 530-536

Conflicts of Interest

The author(s) declare no potential conflicts of interest concerning the research, authorship, or publication of this article.

Contribution of individual authors to the creation of a scientific article (ghostwriting policy)

The author(s) contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

Sources of funding for research presented in a scientific article or scientific article itself

No funding was received for conducting this study.

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