Design and Implementation of a High-Speed D Flip Flop using CMOS Inverter Logic

JAYADEVA G. S., NIKHIL MURALI, MEGHANA S., RAKSHA K. KUMAR, NITHIN ANIL NAIR
Deptartment of Electronics and Communication Engineering,
BMS Institute of Technology & Management,
Bangalore,
INDIA

Abstract— This paper proposes an improvised D- flip flop configuration based on tristate inverter logic, which reduces the power dissipation, decrease the transition time from the input to output as well as reduced time to reach rail to rail voltage. The flip flop uses transmission gate instead of pass transistor to achieve this requirement. The design is simulated using 90nm CMOS technology and data is propagated at 50% duty cycle. The circuit is simulated using Cadence tools to assess the performance with respect to delay and power. These D-flip flops have numerous applications such as buffers, registers, digital VLSI clocking systems, microprocessors etc.

Key-words— D Flip flop, Cadence, Power consumption, Propagation delay.

Received: June 17, 2021. Revised: October 8, 2022. Accepted: November 11, 2022. Published: December 19, 2022.

1 Introduction

In the field of Very Large Scale Integrated (VLSI) circuits, sequential circuits are expansively used and serve a vital role in digital logic design. The purpose of recent circuit designs is to retain or improve the characteristics feature necessary for VLSI industry, while reducing power consumption. There are two major types of power dissipation viz, static and dynamic. The dynamic power dissipation is mainly due to switching activity of the load capacitor. Internal leakage is caused in devices when it is not in the working condition which constitutes the static dissipation [6], [7].

Various attempts have been made to reduce power dissipation using different technologies, with different topologies. Specifically, the dynamic power. Among them CMOS technology with single edge triggering flip-flop topology is popular [1], [2]. Further the devices kept on scaling to reduce individual device power dissipation. At the same time the density of components in a chip increases to accommodate more functionality, which increased the power dissipation in a given chip area.

The CMOS Technology node, in which we essentially deal with the physical dimensions of the device can accommodate more transistors in the given area and also can switch faster and consume less power compared with other technologies, hence require less energy and the chip runs at lower temperature.
The power dissipation and time delay variations depend on various parameters such as supply voltage, aspect ratio, oxide thickness, load capacitance, threshold voltage, which vary as the technology scales down.

In a given CMOS circuit power dissipation can be from three main sources. Namely, Signal transition, short circuit current flowing from supply to the ground terminal, and leakage currents. The short circuit power becomes comparable to the dynamic power dissipation as the technology is scaled down. Furthermore, the leakage power also plays a hugely important role in a digital CMOS circuit. As we further reduce the channel length, gate oxide thickness and threshold voltage in CMOS circuits, the significant contributor to power dissipation turns out to be the high leakage current [3], [4], [5]. Therefore, to estimate and reduce leakage power, relevant modelling and accurate identification of different leakage components is principally important in high-speed and low-power applications. The load capacitance is reduced from 10fF to 1fF to reduce switching capacitance and power dissipation.
CMOS technologies can be used to describe various systems in which CMOS flip-flops are extensively used such as personal computers, servers, other portable systems etc.

This work simulates modified D-ff using 90nm technology with single edge triggering flip-flop topology node on Cadence tools using CMOS technology. The earlier work on D-ff maintains functionality up to 100 Mhz [8] and 1 GHz [3]. Our modified D-ff with single edge trigger works up to 2.5 GHz with much less power dissipation, uses only 1V power supply. In the design of an analog circuit, generally the power dissipation increases with increase in frequency of operation. The aim of this work is to show that with the introduction of transmission gate instead of Pass transistor in D-flip flop (D-ff) results in less power dissipation even with higher frequency of operation.

2 Related Work

The power dissipation can be reduced by reducing capacitance and the supply voltage in CMOS. This may result in the low performance of device. For low power consumption and low power dissipation, various models have been proposed with different topologies and their effect varies on power dissipation and propagation delay [1], [2], one such topology is the Single Edge-Triggered Flip-Flop (SET).

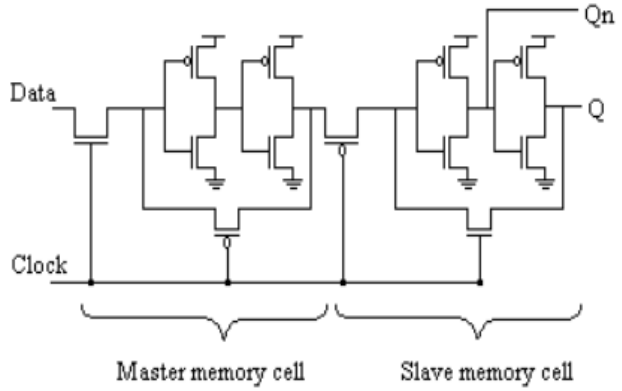

Fig. 1: SETFF Configuration

The advantages of SET flip flop are:

- SET has the fastest delay among any flip flop considered along with large amounts of negative set up time.
- SET uses the simplest flip flop design wherein the sampling data is used only on one clock edge.
- SET shows better results with respect to power dissipation.
- SETs are the best lower power flip flops.

An improvised version of the SET (Single Edge Triggered) Flip Flop is proposed in this paper which includes a resettable functionality. The proposed design uses tristate inverters instead of pass inverters as shown in Fig.1. In transmission gate (TG) arrangement, the combination of both a PMOS and NMOS not only counteracts reduced noise margin, but also decreases switching resistance and static power dissipation which is due to increased threshold voltage, but requires the clock signal and its complement. The proposed design aims to reduce the power dissipation due to both leakage and switching action, while keeping the propagation delay in check.

In the published D-ff design using SET flip flop [1], the pass transistors have higher leakage current, high switching resistance which results in high power dissipation. which can be minimized using transmission gates. Also, transmission gates give better noise margin. This results in improved performance in frequency of operation and power dissipation.

3 Methodology

3.1 CMOS Inverter Technology

The basic working of the project resembles the functionality of a D-ff. To reduce the waste of energy in flip-flops with low data activity, SET flip-flops has been developed. The proposed flip flop (Fig. 2) has the least power dissipation among all the designs for low switching activities

Fig. 2: Flip flop block diagram

The Delay(D) flip-flop is a clocked flip-flop which has a single input ‘D’. The output follows the state of ‘D’ each time a D-ff is clocked. D and Clock are the two inputs for D flip flop.

The given Fig. 3 shows the timing diagram of the proposed design of the D-ff.

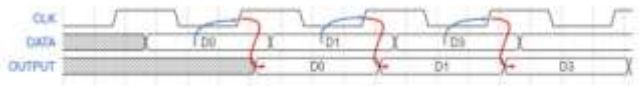

Fig. 3: Timing diagram

As seen in Fig.3, data is passed from the master stage to the slave stage when clock is “0”, and output is seen across Q when clock is “1”.

3.2 Proposed Design

The High-Speed D-ff is proposed to be designed as shown in the Fig.4

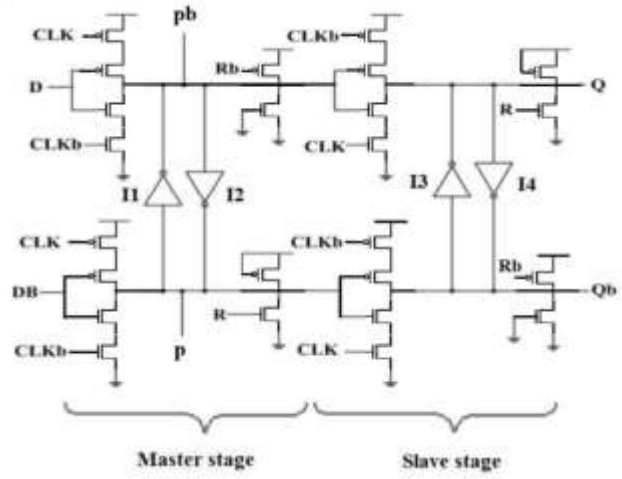

Fig. 4: Proposed design

CLK and CLKb are the clock signals which are complements of each other. D and DB are the inputs, complements of each other. R and Rb are reset signals, complements of each other. Q and Qb represent the outputs.

When CLK is '0', left stage tristate inverters (master stage) are ON and right stage tristate inverters (slave stage) are off. The master stage tristate inverter has been used to implement a switch. At this point, outputs Q and Qb hold the previous value. When CLK rises to '1', the master stage tristate inverters are turned OFF and the slave stage tristate inverters are turned ON, therefore the data is transferred from the master stage to the output on the positive edge of the clock. Meanwhile, the master stage holds the previous value using the back-to-back inverters I1 and I2. So, at the rising edge of CLK, the input data (D) is sent to the output (Q).

The back-to-back inverters act as a memory latch, storing the data when the respective stage is inactive. The reset functionality is added to the D-ff which deactivates the respective master/slave block in that clock signal.
Fig.5 represents the test bench, which include the Design Under Test (DUT) block,

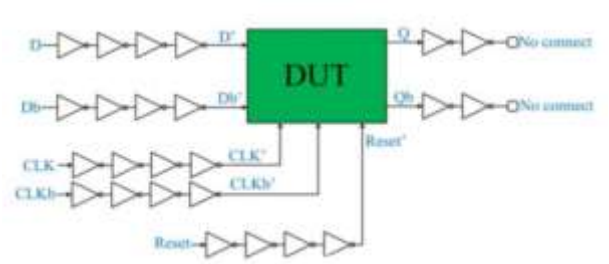

Fig. 5: Test bench

The 4 stage inverters act as buffers for the input and 2 stages at the output signals. The inverters can be used to increase driving strength by changing the strength of the transistors.

4 Results and Discussion

The proposed structure of the positive edge triggered D-ff constructed with the help of Cadence tool. Fig. 6 shows the sole DUT of the D-ff, and Fig.7 denotes the testbench along with its respective input and output environments.

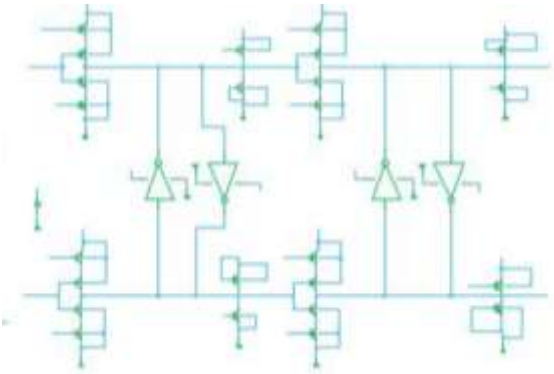

Fig. 6: Schematic of D-ff in cadence

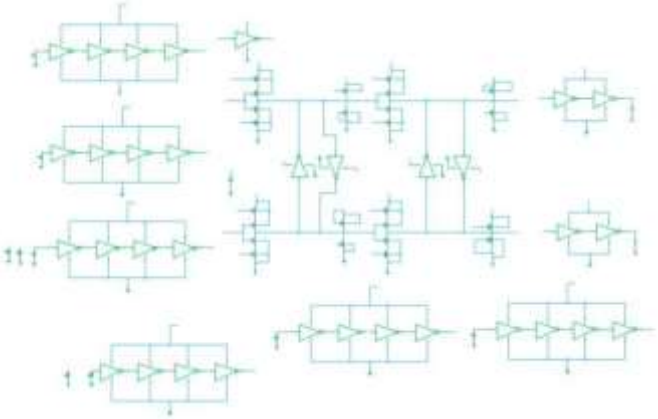

Fig. 7: Schematic of test bench

The pass transistor SET design [1] shown in Fig.1 yielded the following results in Cadence Virtuoso. Fig. 8 shows the waveform of the referred SETFF design using 1Ghz clock frequency.

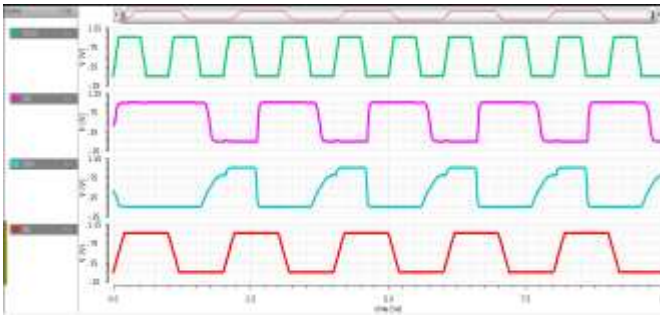

Fig. 8: Waveform of referred design at 1 GHz [1]

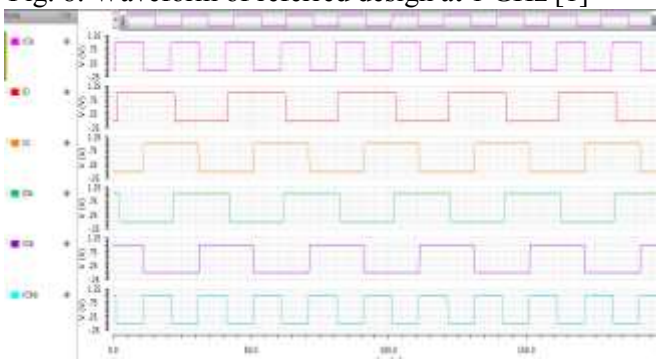

Fig. 9: Waveform of proposed design at 1 GHz

From the Table 1, we see that, the proposed design and the earlier work [1] shows similar propagation delay, but in the proposed design, the power dissipation is reduced approximately by 50% at 1 Ghz frequency. The output waveform shown in Fig. 9, gives the output obtained from re-simulating the design [1], which shows the further degradation as the clock frequency increases above 1 GHz.

Table 1. Performance Comparison of Referred and Proposed designs

90nm, 1V 1Ghz Clock frequency	**Referred Design**	**Proposed Design**
Clock to Output Delay(Tcq)(s)	1.074n	1.076n
Avg Power(uW)	42.32	22.38

The proposed design shows stable results in 2.5Ghz clock frequency as well. The test bench is simulated in nominal voltage temperature conditions i.e., 25°C, 1V as stipulated for 90nm CMOS technology. The functionality is observed in given Fig.10.

The performance of the proposed design at higher clock frequencies is presented in Table 2.

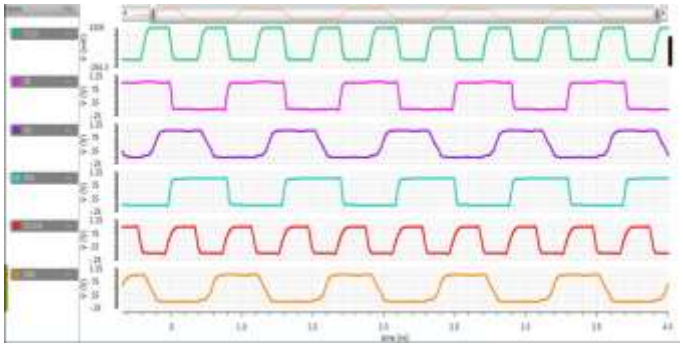

Fig. 10: Functionality check at 2.5 GHz

Table 2. Performance of Proposed Design at Higher Clock Frequencies

Clock Frequency (2.5 GHz) 90nm, 1 V, 25°C		
Signals	**Rise Time (ps)**	**Fall Time (ps)**
D	26.45	26.45
Clk (Clock)	42.99	42.99
Q	72.47	74.05
Delay(Tcq)(s)	475.8 p	
Average power (W)	50.73 u	

5 Conclusion

In this paper we implemented and constructed an improvised low power design using transmission gate instead of pass transistors for implementing D-ff. The results obtained from the implementation show that there is an improvement in stability in higher frequency of operation along with 50% lower power dissipation at 1Ghz frequency. Further, the frequency of operation is enhanced up to 2.5 Ghz giving stabilised output with only an average power dissipation of 50.73uW. The results obtained is promising for sequential circuits. The results were verified using Cadence Tools with 90nm CMOS Technology.

The proposed D-ff design using transmission gate concept can be extended to other sequential circuits and can be further analysed, verified for similar improvement in frequency and power dissipation

References:

[1] Rishikesh V. Tambat and Sonal A.Lakhotiya, "Design of Flip-Flops for High Performance VLSI Applications using Deep Submicron CMOS Technology", International Journal of Current Engineering and Technology, Vol.4, No.2 (April 2014)

[2] Jahangir Shaikh and and Hafizur Rahman, "High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop", International Symposium on Devices, Circuits and Systems (ISDCS), IEEE Xplore 2018

[3] Uming Ko, and Balsara P.T., "High-performance energy-efficient D-flip-flop circuits," IEEE Transactions on Very Large-Scale Integration Systemstion Systems, Vol. 8, Issue 1, Feb. 2000.

[4] Johnson T.A., Kourtev I.S., "A single latch, high speed double-edge triggered flip-flop (DETFF)," The 8th IEEE International Conference on Electronics, Circuits and Systems, Volume 1, 2-5 Sept. 2001.

[5] B.Chinnarao, B.Francis & Y.Apparao, (2012), Design of a Low Power Flip-Flop Using CMOS Deep Submicron Technology, International Conference on Electrical and Electronics Engineering (ICEEE) -9th Sept, 2012, Guntur- ISBN: 978-93- 82208-21-1.

[6] Akash Agarwal, Tarun Kumar Gupta, Ajay Kumar Dadoria, "Ultra low power adiabatic logic using diode connected DC biased PFAL logic", Vol 55, pp.46-47, March 2017.

[7] Manoj Sharma and Arti Noor, "Positive Feed Back Adiabatic Logic: PFAL Single Edge Triggered Semi-Adiabatic D Flip Flop", African Journal of basic and Applied sciences 5(1):pp.42-46, 2013.

[8] Dahlan Abdullah," Design of Set Based D Flip-Flop for High-Speed Applications" Vol. 2 No. 2 (2020): JVCS

Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

-Dr. Jayadeva G. S. has supervised and advised the research activity planning and execution, including mentorship

-Nikhil Murali designed the Methodology and carried out the Simulation in Cadence Tools.

-Meghana S. has organized the Investigations and Visualization of the paper.

-Raksha K. Kumar carried out Management and Coordination responsibility for the research.

-Nithin Anil Nair was responsible for the Formal Analysis of the design.

Conflicts of Interest

The author(s) declare no potential conflicts of interest concerning the research, authorship, or publication of this article.

Sources of funding for research presented in a scientific article or scientific article itself

No funding was received for conducting this study.

Creative Commons Attribution License 4.0 (Attribution 4.0 International , CC BY 4.0)