Design Guidelines for Low Power Embedded Systems using Low Power Electronics

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Abstract: - The design of Low Power Embedded Systems (LPES) and IoT products may include a variety of power management techniques, or they may incorporate sophisticated on-chip capabilities that assist in reduced power usage. The power management and low power consumption of embedded systems are also enabled by complex algorithms, and every Low Power System (LPS) may require a mix of approaches to avoid using extra battery power. There are several strategies we may use when creating an LPES that must be extremely power efficient while simultaneously offering the necessary degree of computational capability. It all depends on the design specifications that must be met. Then, if at all feasible, choose the appropriate low-power components from Low Power Electronics (LPE). After studying and reviewing multiple LPES real-time projects, we compiled a list of a few strategies we may use to approach low-power design and consumption for embedded systems. Following the analysis of numerous LPES real-time projects, we came up with a list of a few approaches to low-power design for embedded systems using LPE. There are additional benefits of LPES design. Less heat is generated through LPES, which is better for the environment. For 1000 LPES devices, one watt of power saved per device equals one KWH i.e. we can save 1 unit of electricity. Design with low power increases the component and system reliability. The embedded system's operating life is enhanced. In many instances, LPES designs may result in a reduction in production costs. The LPE components chosen are more affordable and inexpensive. Hence, the low-wattage power supply, LPES design is easier and less expensive.

Key-Words: - low power embedded system, low power design, low power PCB, low power electronic components, power management, battery management, algorithm optimization.

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1 Introduction

The LPES Design is on the rise. An embedded system's low power consumption is crucial for building a battery-powered device. There isn't a single guideline that applies to all types of use scenarios. System design, circuit design, firmware design, and trade-offs are all mixed together in this situation to develop LPES, [1], [2], [3], [4], [5], [6]. We discuss a few design guidelines for LPES using LPE. These guidelines will be very helpful for designing LPES. Initially, there are two things to undertake before starting the design work on the LPES, [7], [8], [9].

1.1 Be Aware of the Electricity Budget

Know your LPES design's entire power budget. For instance, it should not draw more than 500 mA. It should be well-known how long of a backup period is needed if it is battery-powered.

1.2 Calculate the Electricity Usage

The LPES design should be represented in a block diagram. We can identify the key components and their power requirements using this block diagram. Datasheets and application notes include information about device power consumption.

The LPES design engineer will be able to develop the best power-saving approach to meet the goal with the aid of the power budget and predicted power consumption based on high-level LPES design, [10], [11], [12], [13]. This will also assist the design engineer in determining if the supplied battery capacity is adequate or not (early in the design process). Always take into account the battery's self-discharge and practical capacity when utilizing the battery instead of the capacity shown on the datasheet. There are numerous strategies to save power, but not all of them may be appropriate for all use cases.

2 LPES Design Requirements

Gathering requirements of LPES is the initial step in every effective project design execution. We must create criteria around our need for power efficiency. Prolonging battery life, guaranteeing overall power efficiency and design reliability are likely to be our high goals, [14], [15], [16], [17], [18], [19]. We need to make decisions on a few of the following things to achieve our goals:

• How long can our battery-operated system be deployed before it has to be recharged?
• How much computing power does our system require to function properly?
• What power management strategies or features are supported by our electronic components?
• Are there any high-power consumption circuit blocks or power-hungry peripherals that need intermittent power?

We can devise a plan to create a successful LPES design if we know the answers to these questions. Selecting crucial parts and peripherals that might need to be combined with a power management algorithm is the first step in the design process. We may decide how to best apply a power management plan at the system level once we've selected the crucial LPE components.

The current trend in emerging IoT devices is to incorporate more features into a smaller form factor, while also increasing computing power, wireless connection protocols, and processing speed/memory. More engineers are becoming specialists in High-Density Interconnect (HDI) design, low-EMI stack-up design, RF layout and routing, and other formerly complex areas of PCB design as a result of this trend. Several design teams are also being driven to become acquainted with LPES software packages, operating systems, UI/UX design, and algorithm design as a result of this.

Whatever capabilities your next IoT device has, it must be built with low power consumption, reliable power management with near zero power fluctuations, low conducted and radiated EMI, and lots of sensors/HMI to communicate with the real world. Arguably, the most important of these aspects is Low Power-PCB (LP-PCB) design; if the device can't operate for more than an hour, then it will never last in the market.

3 LP-PCB Design for LPES

LP-PCB design entails more than just selecting electronic components with low power consumption, however, this is a significant design consideration. Our design should begin with the power supply since it is the most essential predictor of usability. Is our LPES battery-powered or do we need a wall outlet? How long will it run on battery power before needing to be recharged? When choosing hardware, this ought to be the initial place to look. Some designers prefer to work in the opposite direction. It is critical to select processing power and memory (RAM and Flash) to ensure that the LPES program can operate with the lowest computation time. This will further restrict your system's power requirements, but it may impair functionality. The LPES mobile gadget to be created may not be mobile since it requires regular recharging, a huge battery, or continual wall power.
Our next LPES, the LP-PCB design for an IoT device will almost certainly have many DC-DC converters. The upstream regulator must be directly connected to our power source and can be utilized to control DC-DC converters. These IoT converters typically operate at the order of hundreds of kHz to a few MHz. They can be an issue for both radiated and conducted EMI. The LP-PCB stack-up design is critical for shielding and reducing radiated emissions. It prevents switching noise from interfering with downstream components. And validate that the electrical component is in the correct location.

LPES active devices (MCUs, FPGAs, SoCs/SoMs, and any other IC that processes or manipulates data) should be selected such that they only give the necessary processing capabilities while consuming the least amount of power. Several MCUs that provide processing power for data-intensive applications, as well as other SoCs for signal processing and other functions, have a sleep mode. When a component enters sleep mode, it effectively halts and uses the least amount of power while waiting for a wake-up notification.

Once we've determined the size of our battery, maximum power consumption, and needed supply voltages in various components, we must choose components that deliver steady power as the device functions. Steady power is a key aspect of power integrity in LPES, while it is closely tied to EMI issues both within and outside the device, as well as signal integrity. Addressing all of these problems at once necessitates making the proper PCB design choices. This comprises LP-PCB stack-up design, power delivery block network design, and routing and layout isolation. The LP-PCB stack-up design, layout, and routing are explored below.

3.1 LP-PCB Stack-up Design Selection for LPES

The LP-PCB stack-up will play a significant role in LPES power integrity and isolation in designs. A minimum of six layers will be used in advanced LP-PCB design for LPES IoT devices. PLDs with a high pin count on densely packed boards can easily span several dozen layers. To meet our form factor needs, we may employ a flex or rigid-flex board for LPES. For example, the latest iPhone employs over two dozen flex boards to make place for a bigger battery.

The main problem in developing LP-PCB stack-up is giving an area for stripline routing and placing our power and ground planes on nearby levels, regardless of how many layers we include in the board.

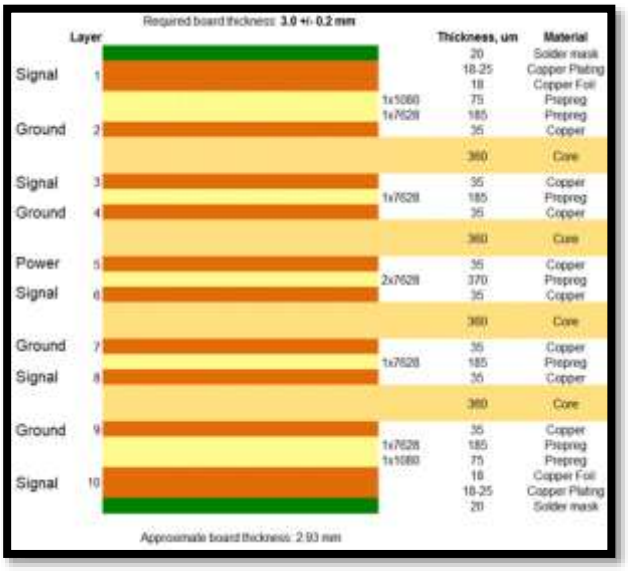

Fig. 1: Sample of 10-layer firm stack-up guaranteeing the power integrity in IoT/mobile device LP-PCB design for LPES.

Figure 1 depicts one of the LP-PCB stack-up designs for LPES. It is beneficial for a variety of factors. The neighboring power and ground planes will have a sizable interplane capacitance even on a typical 1.57 mm board. It aids in lowering the power delivery block network of the LPES design's overall comparable impedance. We should have a very stable power distribution in this board with negligibly low ringing once a few decoupling capacitors are added for key components. We might prefer working with a greater layer count on a thinner board if we are working at lower signal levels. This will increase interplane capacitance and bring the power and ground planes closer together. Second, stripline routing is possible in inner layers thanks to the arrangement of alternating ground planes and signal layers. The nearby ground planes will offer a short return route with a low loop inductance, providing shielding and aiding in the reduction of ringing.

Another thing to think about is routing between LP-PCB layers, particularly as the board's component and trace density grows. HDI design techniques gain appeal as more devices achieve higher densities. Traces themselves don't alter much in terms of design, but fanout techniques for high pin-count components and via design do. The two main choices when creating a fanout plan are dogbone fanout and via-in-pad. Figure 2 below depicts three potential variations for fanout/escape routing.

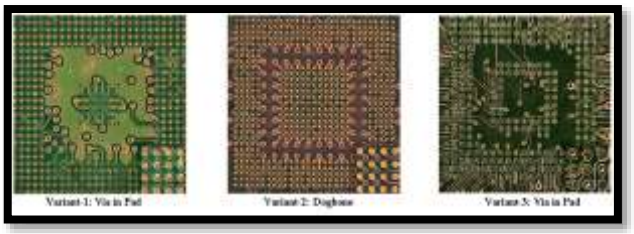

Fig. 2: Approaches for HDI fanout for high-density BGAs in LP-PCB design for LPES.

3.2 LP-PCB Design and EMI/EMC

Only through the filtration process, we can effectively fight conducted EMI from switching noise in LPES PCB designs. Switching noise on a regulator circuit is significantly decreased by the output capacitance. However, switching regulators also generate radiated EMI, which can cause a nearby device to experience a significant voltage change. Switching regulators/converters that generate a few Amps of current can cause a neighboring circuit to generate a few Volts of noise. Where a switching regulator induces voltage, vias, and circuits with high loop inductance can pose challenges.

The LPES power converter circuitry should be positioned farthest away from the most delicate circuits, antenna components, analog circuitry, and any other digital signals that operate at a low level (less than 3.3 V). This will make sure that any emitted EMI that does get to these components, causes less noise to be produced. Where to position the output inductor and input/output capacitance for converter ICs is another thing to think about. These shouldn't be routed through vias and should be positioned as near to the converters as feasible. The input/output capacitors are an important caveat. To minimize loop inductance, the ground pin on these capacitors needs to be routed through a via and back to the neighboring ground.

To reduce radiated EMI between the power section and antennas, analog circuits, and any other components that operate with low supply voltage, we should consider using some shielding methods in severe LPES PCB design situations when dealing with an IoT/mobile device that provides high current. Can shielding be one solution? The power control portion of the LPES PCB can readily be housed in grounded shielding cans. Figure 3 shows the shielding for mobile and IoT devices that maintain power and transmission fidelity. The other choice is to use ground pour and via barriers to separate various functional blocks; this approach may be most effective with miniature form factor flex/rigid-flex boards. Typically, they are made to produce an image charge at a particular frequency. Ground pour, on the other hand, will offer broadband shielding and separation but attenuation. Verifying isolation methods and ensuring that any induced noise does not surpass noise margins in circuits will require the use of some LPES PCB design post-layout simulation tools.

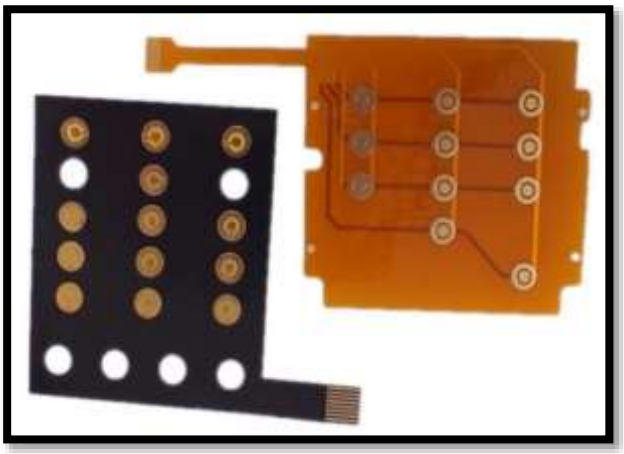

Fig. 3: IoT/mobile device shielding to safeguard the power/signal integrity.

4 LPES Component Selection

The power consumption is greatly influenced by the LPES components like the primary CPU, analog front-end, and peripherals like monitors, and displays. Numerous processor units (MCUs, FPGAs, MPUs, etc.) and other components are expressly advertised as low-power devices, and they can make it possible for LPES to employ a novel power management strategy. Here are some guidelines we may use to design LPES power system architecture when choosing components.

4.1 Begin with Necessities

A certain processor or peripheral might be one of the critical essential components. Find the lowest power alternative that meets the essential functional criteria of that component.

4.2 Peripheral Architecture

Consider the interactions between peripheral blocks, the host processor, and the environment. Incorporate this knowledge to design your LPES architecture.

4.3 Interfaces and Receivers

I2C, SPI, GPIO, and other low-speed digital protocols can all have various power outputs. To use less power overall in LPES, receivers and converters like ADCs may be made to operate at a lower sample rate.

4.4 Devices with Sleep/Hibernate Modes

In LPES, some critical CPUs and other low-power IC blocks include sleep modes. The current is only delivered to important functional blocks. In these modes, the current can fall considerably below 0.01 mA to reduce power consumption and leakage.

4.5 Power Control

After choosing each essential LPE component, it's time to consider power regulation. Opt for the power regulation method with the maximum possible efficiency. Power conversion efficiency may be maintained at levels much above 95% by carefully designing the regulatory phases of LPES.

5 Power Management Techniques

By selecting the proper components of LPES, component-level power usage is simple to handle. However, there are circumstances in which a specialized high-power component is a must in our system. The system should now be built with battery charge management, algorithm optimization, and the ability to toggle on and off specific peripherals.

5.1 Peripherals

One method for ensuring that power is only utilized when it is required is for the host controller to switch peripherals on and off as needed. When a component is not actively processing data, it may accomplish this on-chip, turning off groups of interfaces and lowering the core voltage. Figure 4 represents the block diagram view of power to peripherals managed by switching with a bus topology. Note that this might require digital/analog switch components. Many inexpensive MCUs of

LPES have this functionality, which is very popular. However, there could be system blocks that are not directly linked to the master processor at the system level. Simply shutting off power to the peripheral block or placing a slave CPU in sleep mode might turn them off.

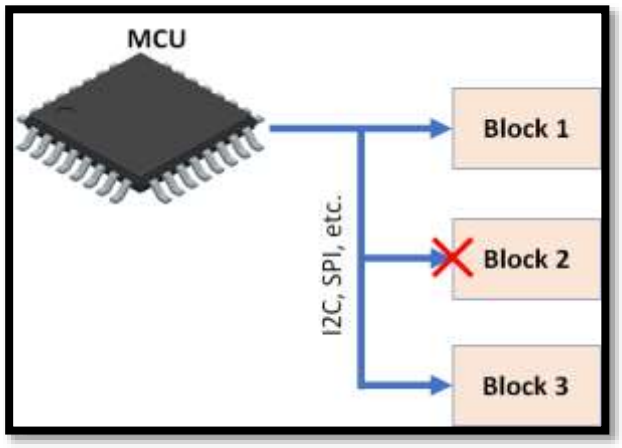

Fig. 4: Power to peripherals can be managed by switching with a bus topology. Note that this might require digital/analog switch components.

5.2 Battery Management

Not all battery packs will support this tactic, however, it is beneficial for multi-cell battery packs connected in series. Implementing a battery management algorithm with a balancing mechanism is one technique to ensure the charge is spread equally across cells and avoid excessive power from being extracted from a single cell. The Texas Instruments BQ769x0 series is one potential component for putting a standard balancing algorithm into practice for LPES design. A microcontroller, FPGA, CPU, or MPU may balance low current across cells with little power loss in this LPES design strategy.

5.3 Algorithm Optimization

Designers of LPES should make sure that any specialized algorithms in their firmware are optimized to reduce computation operations. Enterprise-level software developers frequently have to take into account how many logical operations are required to execute an algorithm and must look for ways to reduce the number of operations required to accomplish a computational activity.

The same is required of LPES firmware and software developers for their respective systems. Lowering the algorithm complexity reduces the host processor's power requirements. The CPU will run fewer tasks for the operation. Hence, it uses less power if background activities and services are removed, along with any unneeded computing operations.

6 Conclusion

In this paper, we presented some of the recent research work being carried out in the field of Low Power Embedded Systems (LPES). We present the basic design guidelines for LPES using Low Power Electronics (LPE). It covers practical techniques on key low power issues such as design requirements, PCB selection, LPE components and I/O considerations, sleep/wake-up issues, power management, and general design issues. There are several strategies to save power, but not all of them are appropriate for every application. However, the designers would be able to reduce the real power for LPES in most of the defined cases. He will be able to develop a successful LPES following the described design guidelines of LPE. He must employ power management strategies, make wise selections when selecting LPES components, and follow crucial design guidelines while designing LP-PCBs.

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