Implementation of Ripple Carry Adder and Carry Save Adder using 7nm FinFET Technology

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Abstract: - The semiconductor industry's continuous effort to miniaturize and be more powerful to increase the overall performance. This has led to the use of FinFET technology for packing more transistors into a smaller space and using power more efficiently compared to planner MOS technologies. Compared to the MOS technology, FinFET technology provides better advantages such as improved transistor performance, lower leakage currents, and enhanced power efficiency. The proposed work includes integrating fundamental components like the NAND gate, 2:1 MUX, and full adder (FA). These components are combined to build both Ripple Carry Adder (RCA) and Carry Save Adder (CSA). The work is carried out using 7nm FinFET technology and this research involves a thorough analysis of power consumption and propagation delay, with the implementation carried out using the Cadence Virtuoso tool. The study highlights the improved performance of 7nm FinFET technology compared to MOSFETs.

Key-Words: - RCA, CSA, Technology Scaling, 7nm FinFET technology, Average power, propagation delay, Circuit Optimization Techniques, MOSFETs, cadence virtuoso.

Received: March 27, 2023. Revised: November 8, 2023. Accepted: December 13, 2023. Published: December 31, 2023.

1 Introduction

Fin Field-Effect Transistors as FinFETs, are the type of transistor used in semiconductor technology for integrated circuits which includes microprocessors, memory chips, and other electronic devices. They are a fundamental component of modern semiconductor manufacturing processes and offer several advantages over the MOSFET transistor designs.

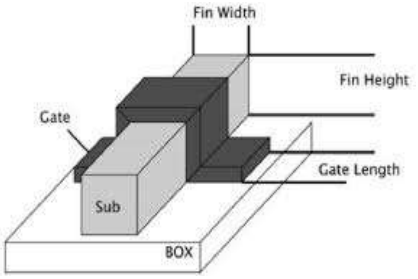

Fig. 1: FINFET Structure

FinFETs exhibit a distinctive three-dimensional configuration characterized by a slender silicon "fin" that stands vertically from the silicon substrate as shown in Figure 1. This fin serves as the tangible path through which electric current passes between the source and drain terminals. The gate is isolated by the fin and surrounded by the oxide layer of very thin dimensions, [1]. To elaborate, there exists a 3D solid channel that is physically present between the source and the drain. The most important and major challenge associated with MOSFETs is the leakage current, this issue is addressed via FinFETs through their unique structure. In FinFETs, the gate covers the sides and top of the fin, increasing the control over current flow compared to planar MOS transistors.

This type of design has the greater advantage of reducing leakage current when the transistor is in the off state. Thus, improving the overall efficiency and are best suitable for battery-powered devices like smartphones and laptops. These FinFETs offer improved performance characteristics compared to planar transistors as they offer faster-switching speed, allowing for higher clock speeds in microprocessors and faster data transfer in memory chips.

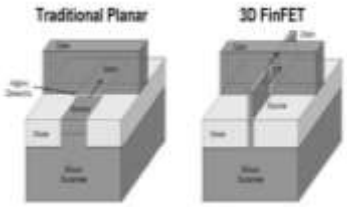

Fig. 2: Comparison between MOSFET and FinFET

To strictly follow Moore's law, extensive scaling of MOSFETs has come into the picture from the past four decades which in turn resulted in an overwhelming increase in the performance of modern-day integrated circuits, [2]. The FinFETs have a greater scope over the scaling of transistor sizes, leading to smaller and more power-efficient ICs. The 7nm, 5nm, and even smaller FinFET technology nodes have been achieved. Which can't be seen in planar transistors. The nominal supply voltage used was 0.7V, [3] or even 0.2V for FinFET technology. Nowadays FinFETs have become the industry standard for advanced semiconductor processes. Companies like Intel, TSMC, Samsung, and Global Foundries have adopted FinFET technology in their manufacturing processes.

The excellent gate control abilities of the channel, and multiple-gate devices such as surrounding-gate transistors represent the most promising solution to replace conventional bulk transistors, [4]. In Figure 2, the FinFETs are vertical structures whereas the MOSFETS are horizontal structures. Hence the rate of current flow will remain the same no matter with scaling down in the channel length. The planar conventional metal-oxide semiconductor field effect transistor cannot be scaled down below 20nm, [5], but, FinFETs overcome this limitation by introducing a three-dimensional fin-like structure instead of the traditional planar design.

The FinFETs are an example of multi-gate transistors, which have multiple gates controlling the channel. This design improves performance and provides better control over the behavior of the transistors.

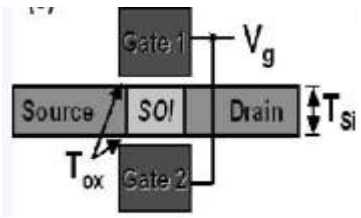

Fig. 3: Double Gate FINFET Structure

The basic architecture and mode of operation of a FINFET do not differ much from traditional field effect transistors. A source and a drain contact are present, with a gate in between to regulate the current flow. However, Figure 3 illustrates the incorporation of multiple gates. In this figure, two gates are positioned vertically, a configuration implemented to mitigate current leakage. Even in the few cases where three gates exist, the Sol is replaced by one more gate. Channel which is very thick such that the gate has great control over carriers within it.

There exist two types of structure depending upon the gate arrangement: insulated gate and short gate FinFETs. In this work, a SG (short Gate) FinFET is used. It consists of three terminals (3T), here the front and back gates are shorted (connected) these 3T include source, drain, and a gate terminal with a Fin that connects both source and drain as in Figure 4. The threshold voltage cannot be controlled externally. It occupies less area compared to IG so, in the majority of the time SG is preferred.

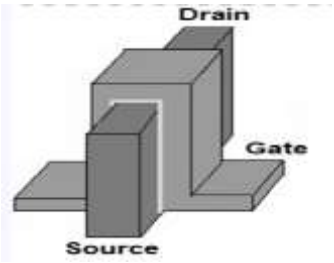

Fig. 4: Structure of SG FinFETs

Although FinFET technology has brought many advances, such as less power consumption, it has also brought some challenges, [6], like complex fabrication processes, strain sensitivity, variability, heat dissipation, etc.

The literature survey is presented in section 2. The details regarding the proposed method are discussed in section 3. The results are discussed in section 4. Finally, section 5 is regarding the conclusion and outlines future work.

2 Literature Survey

In this work, [6], authors have developed a digital circuit 3-2 adder compressor (AC) which can withstand variations in three key factors: process, voltage, and temperature (PVT) and mainly focused on the verification part rather than design. In this study, it is determined that

the circuit can operate within the specified range, considering the key parameters mentioned earlier. The investigation is conducted within the context of a specific semiconductor technology called ASAP7, which is designed for the 7nm FinFET technology node. This study utilizes an academic-oriented Process Design Kit named ASAP7, jointly developed by Arizona State University and ARM. The circuit was designed in cadence virtuoso by following a ten-step design flow, including defining transistor parameters, technological models, and physical design in the same tool. Further, they built a layout where it undergoes verification steps, which include a Design Rule Check, Layout versus Schematic, and parasitic extraction. using Cadence Virtuoso tools. Further, a SPICE-level netlist is generated according to the layout, including parasitic effects, for more accurate electrical simulations. Finally, it is concluded that the variation of supply voltage by ±10% from the nominal value (700mV) and the study evaluation of the circuit's performance across a range of temperatures, from -50°C to 125°C is the range in which the circuit operates in an optimum way.

The authors of this paper primarily discuss choosing between multi-level logic design (using multi-leveled gates) or employing complex gates. The goal is to minimize the impact on the output when subjected to either transient faults or process variability effects. The process variability effects are those errors that are caused in building the circuits at the base level architecture (slight differences in the dimensions, electrical properties, and performance characteristics of individual components) and the transient faults that are unpredictable errors or malfunctions that can occur. Two topologies are designed using the 7nm FinFET technology at the layout level. Additionally, the conclusion is drawn that multi-level arrangements exhibit a 50% reduction in sensitivity to transient faults and are at least 30% more resilient to the effects of process variability, [7].

This paper, [8], provides information regarding two modules of the Manchester Carry-Chain Adder, which utilizes both NC-FinFETs and standard FinFETs technology. The adder is calibrated with 14-nanometer FinFET technology. The model captures short-channel effects like subthreshold swing (SS) improvement, VT roll-up, and the inverse Vds-dependence of VT with decreasing gate length. The conclusion is made that NC-FinFET-based adder could significantly reduce switching energy by 60% compared to FinFET-based adder.

3 Methodology

There is a crucial need for the development of circuits that consume low power and operate at high speeds, [9]. The Adders are the basic building blocks of any electronic circuit. The implementation of an RCA and CSA utilizing 7nm FinFET technology represents a proposed approach. The proposed RCA and CSA in this project share similarities with conventional designs, but distinctions arise from modifications in the library and other tool-specific changes. An RCA typically comprises multiple, FA units, with each FA adding two bits 'a,' 'b,' and 'carry-in,' resulting in a sum and a carry-out. This configuration serves as a fundamental digital circuit for binary addition in electronic devices and computers. Its key merit lies in its simplicity, making it a widely adopted choice for small to medium-sized adders. The implementation of ripple carry adders is uncomplicated, requiring minimal hardware resources and straightforward logic, as illustrated in Figure 5.

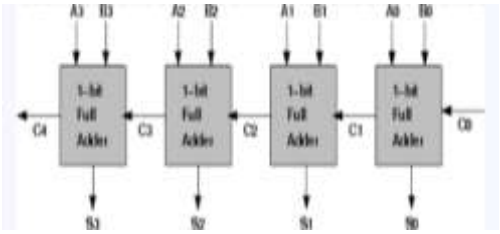

Fig. 5: RCA

Each full adder (FA) produces both a sum bit and a carry-out bit. The sum bit plays a role in determining the final 4-bit result, whereas the carry-out bit is forwarded to the next FA in the sequence. A significant advantage lies in their testing and debugging simplicity. As each full adder stage functions independently, the verification process is streamlined, and any errors are confined to individual stages, facilitating a more straightforward troubleshooting process.

A Carry-Save Adder (CSA) is a digital circuit designed for the rapid addition of multiple binary numbers. In this configuration, each full adder receives three inputs: two bits for addition and a carry-in, as depicted in Figure 6.

The output includes a sum and a carry-out. To add multiple numbers using this CSA, the process involves two stages.

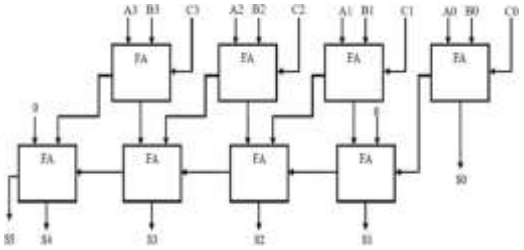

Fig. 6: CSA

Initially, intermediate results are generated using full adders, with the carry-out from one FA serving as the carry-in for the next. In the second stage, the carry-out from the last full adder contains the most significant bits of the result, while the sum outputs from all full adders contribute to the least significant bits. This approach minimizes the number of stages compared to ripple-carry addition, leading to a more efficient addition of multiple numbers.

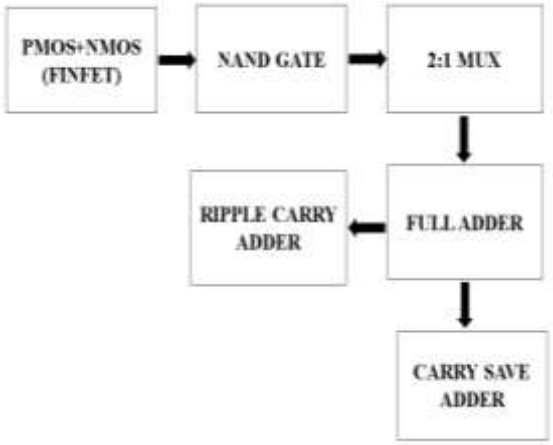

Fig.7: Block Diagram of Proposed Module

The implementation part begins firstly with the design of two input NAND gates using pmosfet and nmosfet. Using NAND gates (four gates among which one acts as a NOT gate, as its two inputs shorted) a 2:1 MUX is developed. At the later part, FA is implemented using the 2:1 MUX. Finally, the RCA is built utilizing these full adders which efficiently perform the addition and provide sum as well as carry. Similarly a carry-save adder is built using full adders as in Figure 7.

4 Results

The simulation of the proposed work is conducted using the Cadence Virtuoso tool, yielding the following outcomes, Figure 8(a), and Figure 8(b) illustrate the symbolic representation and output of a NAND gate constructed with 7nm FinFET technology. The resulting output is notably precise and sharp when compared to CMOS technology.

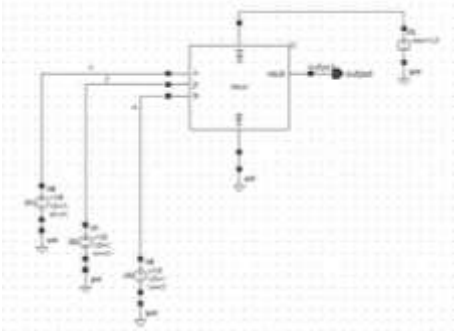
Fig. 8(a): Symbolic representation of NAND Gate

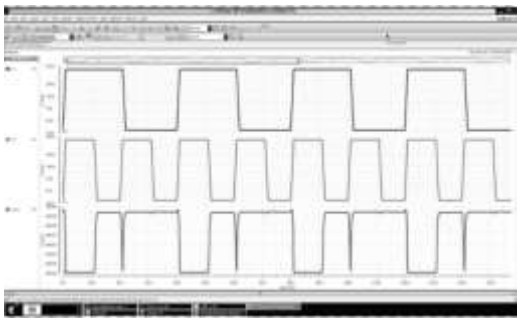
Fig. 8(b): Output representation of NAND Gate

Utilizing a NAND gate, a 2:1 multiplexer is constructed, employing four such NAND gates. Within this configuration, one of the NAND gates is transformed into a NOT gate by shorting its inputs, as depicted in Figure 9(a). The resulting output waveform is presented in Figure 9(b).

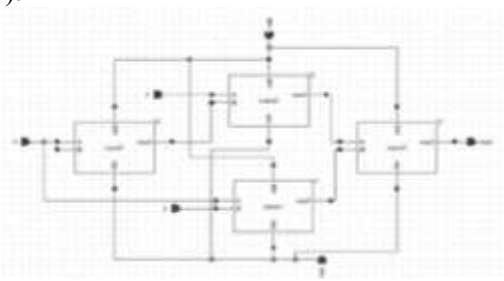
Fig. 9(a): Symmetric of 2:! Mux

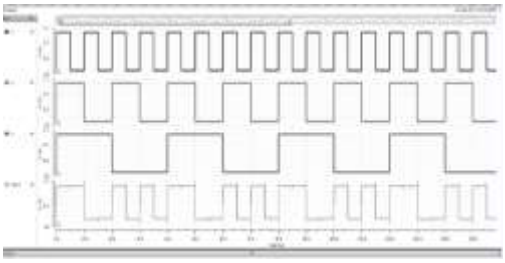
Fig. 9(b): Output of 2:1 Mux

In Figure 10(a), the implementation of a full adder is depicted, achieved through the utilization of a 2:1 multiplexer and a NOT gate, with the necessary connections established. The corresponding output representation of the full adder is illustrated in Figure 10(b).

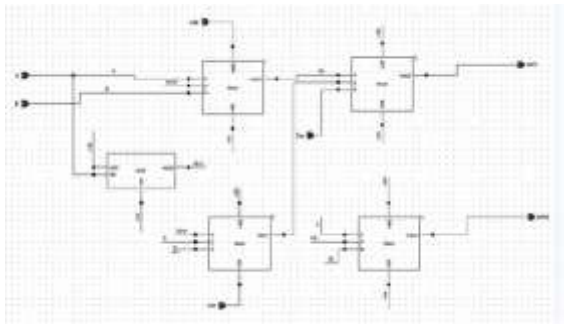
Fig. 10(a): Symmetric of FA

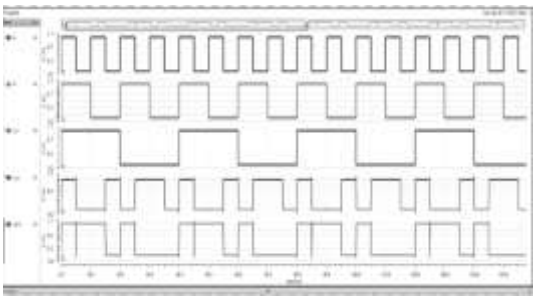
Fig. 10(b): Output of FA

The RCA is assembled using four FAs, as shown in the preceding Figure 11(a). The carry-in (Cin) for the first full adder is set to zero, and all subsequent carries are propagated to the next stage. The output representation of the RCA is presented in Figure 11(b).

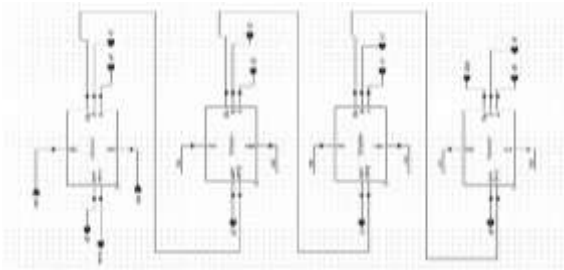
Fig. 11(a): Symmetric of RCA

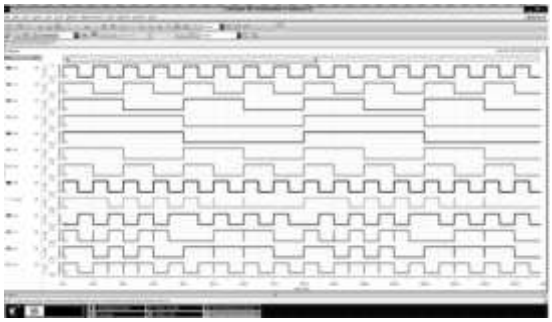
Fig. 11 (b): Output of RCA

The construction of the CSA involves eight FAs, as depicted in Figure 12(a). The output representation of the CSA is presented in Figure 12(b).

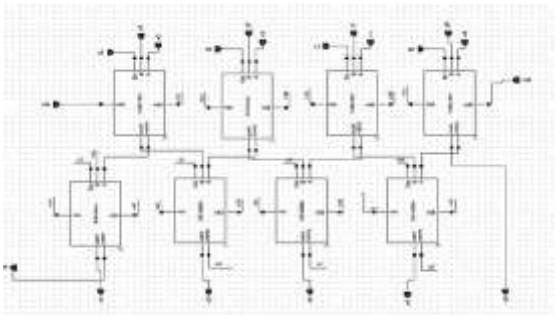
Fig. 12(a): Symmetric of CSA

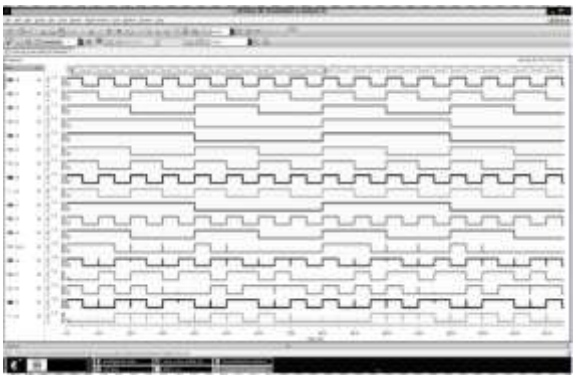
Fig. 12(b): Output of CSA

Table 1. Average Power, Propagation Delay Analysis

Logic Circuit	Average Power	Propagation Delay
Full Adder	3.99.0E-9W	1.1483ps
Ripple Carry Adder	1.596E-6W	5.0085ns
Carry Save Adder	114.1E-6W	5.0072ns

The tabulated values for both the average power and propagation delay of the proposed adders are provided in above Table 1.

5 Conclusion and Future Work

The implementation of a 4-bit ripple carry adder and carry save adder using 7nm FinFET technology underscores their consistent and precise performance across a diverse range of input combinations, affirming their reliability. These adder circuits were specifically designed to ensure accurate binary addition and demonstrated reliability across a variety of input scenarios. Furthermore, considering the potential integration of these advanced adders into complex industrial electronics applications like digital signal processors or microprocessors, Image and signal processing, and so on, their superiority over traditional MOS technology becomes evident. Exploring the utilization of RCA and CSA in emerging domains such as quantum computing or neuromorphic computing offers exciting prospects for advancements in the realm of digital circuit design. Apart from this, it can also be a part of AI, especially in the optimization and enhancement aspects like Optimization using Expert Systems, Fault Diagnosis, etc.

Acknowledgement:
The authors would like to acknowledge the Ministry of Electronics and Information Technology (MEITY) for the support under “Chips to Startup (C2S) Programme.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The first author formulated the idea, and carried out a literature survey, while the second author provided the method, carried out simulations, analyzed and wrote results and a discussion section. Both authors have read and approved the manuscript.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself.

No funding was received for conducting this study. The Ministry of Electronics and Information Technology (MEITY) provided support for the tools.

Conflicts of Interest

The authors have no conflicts of interest to declare.