# CMOS Comparator Design using 90nm Technology

VASUDEVA G[1], BHARATHI GURURAJ [2], MALLIKARJUN P Y[3],
NAGARAJ M LUTIMATH[4], TRIPTI R KULKARNI[5]

[1,5]Department of ECE, Dayananda Sagar Academy of Technology and Management, Bangalore-560082, INDIA
[2]Department of ECE,KSIT, Bangalore, INDIA
[3] Department of ECE, Dayananda Sagar Academy of Technology and Management, Bangalore-560082, INDIA
[4]Department of CSE, Dayananda Sagar Academy of Technology and Management, Bangalore-560082, INDIA

*Abstract*: In many digital circuits the parameters gain and offset voltage are calculated. In our design of CMOS comparator with high performance using GPDK 90nm technology we optimize these parameters. The gain is calculated in AC analysis and also we measure area, delay, power dissipation, slew rate, rise time, fall time. The circuit is built by using PMOS and NMOS transistor with a body effect and we also measure mobility variation and channel length modulation based on the second order channel effects. A plot of gain and offset voltage also discussed in the paper. Finally a test schematic is built and transient analysis for an input voltage of 1.2V is measured using Cadence virtuoso.

*Keywords*: CMOS Comparator, Offset voltage, Gain, cadence virtuoso, slew rate

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## 1. Introduction

In modern telecommunication systems low power, high speed and high performance ADCs are main building blocks[1] .This ever growing application of portable devices make the power consumption a very critical constraint for circuit designer[2]. Comparators are widely used in ADCs, data transmission, switching power regulators and many other applications[3]. The comparator design plays an important role in high speed ADCs[4]. Power consumption[5]and speed are key metrics in comparator design. For all high speed ADCs regardless of the architecture, one of the critical performance limiting building blocks is the comparator, which in large measure determines the overall performance of data converters[6]. In conversion of analog signal to digital signal comparator plays very important role and influences the overall performance directly[7]. In high speed ADC, speed limiting element is comparator[8]. The comparatoris a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison[9]. The comparator is widely used in the process of converting analog signal to digital signals. In the analog to digital conversion process, it is necessary to first sample the input[10]. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal[11]. If the + VP, the input of the comparator is at a greater potential than the –VN input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the – input, the output of the comparator is at logic 0.In pipeline A/D converter, internal comparator must amplify small voltage into logic levels[12]. The Symbol of comparator as shown in figure 1.

In the proposed design pre-amplifier circuit that amplifies very weak signal it is considered to be the input stage of the proposed comparator. Latch stage is used to determine which of the input signal is larger and amplifies their difference. Clock is used to indicate output level; whether its differential input signal is positive or negative[24]. In order to provide maximum offset voltage we provide reference voltage to the circuit. Output buffer stage is used to convert the output of the latch stage circuit into a logic signal[25].

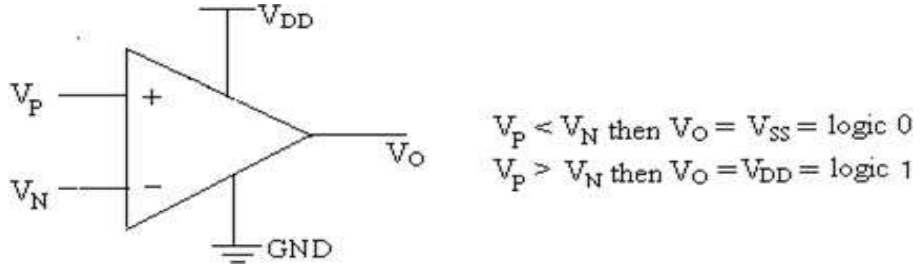


**Fig 1: Basic comparator circuit**

## 2. Related Work

Behzad Razavi and Bruce.A.Wooley[1] described precision techniques for the design of comparator used in high performance Analog-Digital converters employing parallel conversion stage. Here introduced a number of comparator techniques for use in parallel Analog-Digital converters that are implemented in BiCMOS and CMOS VLSI technologies [2].

Lauri sumanen, Mikko Walteri, Kari halonen[2] Described and proposed a new fully differential CMOS dynamic comparator topology suitable for pipeline A/D converters with low stage resolution[14].Here proposed topology, based on switchable current sources, has a small power and area dissipation. The main benefits of the pipeline A/D converter architecture are its capability to a high resolution and very high bandwidth with low power consumption in a small area [2].

R.Lotfi, M.Taherzadev-sami, M.Yaser Azizi and O.Shoaei,[3] describe a 1-V fully differential low power MOSFET only comparator with rail-to-rail input swing is presented which can be suitably used in very low voltage, low power pipelined A/D converters. This comparator utilizes a resistive divider configuration with a MOSFET only clock booster to supply a higher voltage for the dynamic latch in theintervals that a comparison is to be made .

M. B.Gnermaz, L.Bouzerara.A.Slimane, M.T.Belaroussi, B.Lehoudj and R.Zirmi[4]describes and analyzes a low power and high speed differential comparator. This comparator is based on the switched capacitor network using a two phase nano overlapping clock. The offset voltage of the designed comparator has been reduced by means of an positive feedback. Here presented clocked comparator circuit which consist of a pre amplification stage followed by a positive feedback stage forming the latch[4].

Riyan Wang , Kaichang Li, Jianquin Zhang, Bin Nie presented a high speed and high resolution comparator intended to be implemented in a 12 bit 100MHz pipeline analog to digital converter for frequency wireless local area network application. Here the designed comparator presents a rail-rail input range pre amplifier without any capacitance required [5].

Anand Mohan, Aladin Zayegh , Alex Stojceski, and Ronny Veljanovski , Presented the design and implementation of a high speed, low power CMOS comparator as part of an ultra fast reconfigurable flash analog to digital converter for a direct sequence, spread spectrum based ultra wide band radio receiver. Here Ultra means of communication has been around for decades [6].

## 3. Design and Analysis

In the pre-amplifier stage input voltage Vin=1.2 V we get an amplified output also we include transconductance gm in the circuit[13]. In the preamplifier stage Idc=10μA because of drain saturation current the preamplifier works in saturation region, where Vds= β/2 (Vgs-Vt)[14]. By using a clock and providing offset voltage from the clock the output of the preamplifier stage compares both input voltages Vin+ and Vin- and produce an output same as Vin+ - Vin-[15]. The substrate terminal

of PMOS connected to Vdd[16] and substrate terminal of NMOS are connected to the ground. Vin+ =1.2 V provides an input voltage [17] to the NMOS transistor and result in an output voltage which is the difference between Vin-. The preamplifier circuit also acts as a current mirror circuit two PMOS and 2 NMOS transistor we use a clock circuit to provide a dc offset voltage[18].

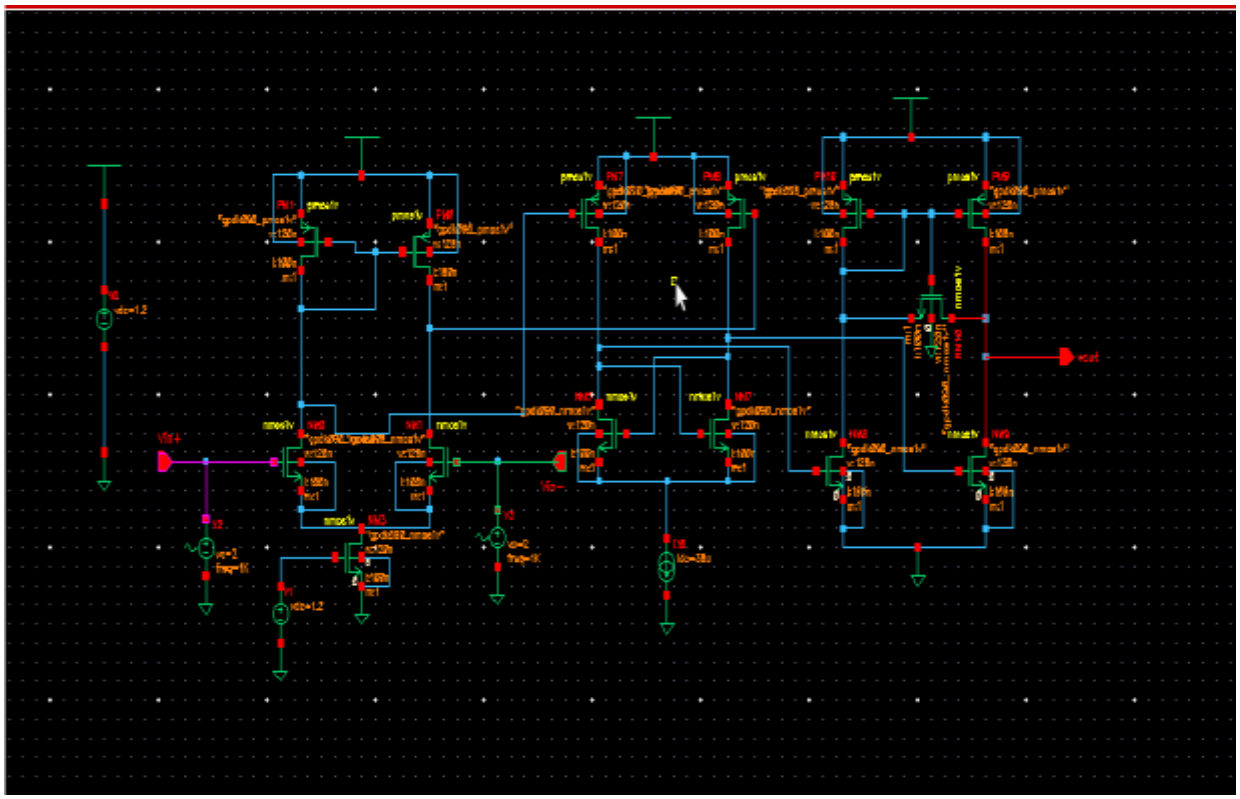

**Fig 2 Schematic diagram of CMOS comparator**

In the latch circuit the PMOS and NMOS circuits are connected in antiparallel which found a common source stage usually in the latch circuit the output of the preamplifier is taken[16] as the input for two PMOS transistor when clock is high the comparator starts to work during this operation the commonsource stage produces the transconductance gm [17]which approximately equal to 1/β. The gate of the NMOS transistor are connected to the drain of the PMOS transistor which reduces the second order effects[18] such as channel length modulation, body effect, and mobility variation also in this stage the feedback[19] is given to the preamplifier stage which reduces the noise from the signal[20].

In the output buffer stage[21] we supply clock frequency of 100MHz which reduces the offset voltage in terms of milli volts. The power dissipation which includes static and dynamic power[22] dissipation are calculated from the output buffer stage[23]. Finally an amplified output is obtained from the output buffer stage which is free of noise variations.

We also calculate slew rate, area, power dissipation, delay, rise time, fall time, offset voltage andgain of the comparator.

## 4. Result and Discussions

From the proposed design of high speed CMOS comparator, designed using cadence virtuso withGPDK 90nm technology is discussed below.

The transient analysis for CMOS comparator is obtained and the input voltage Vin=1.2V is given below

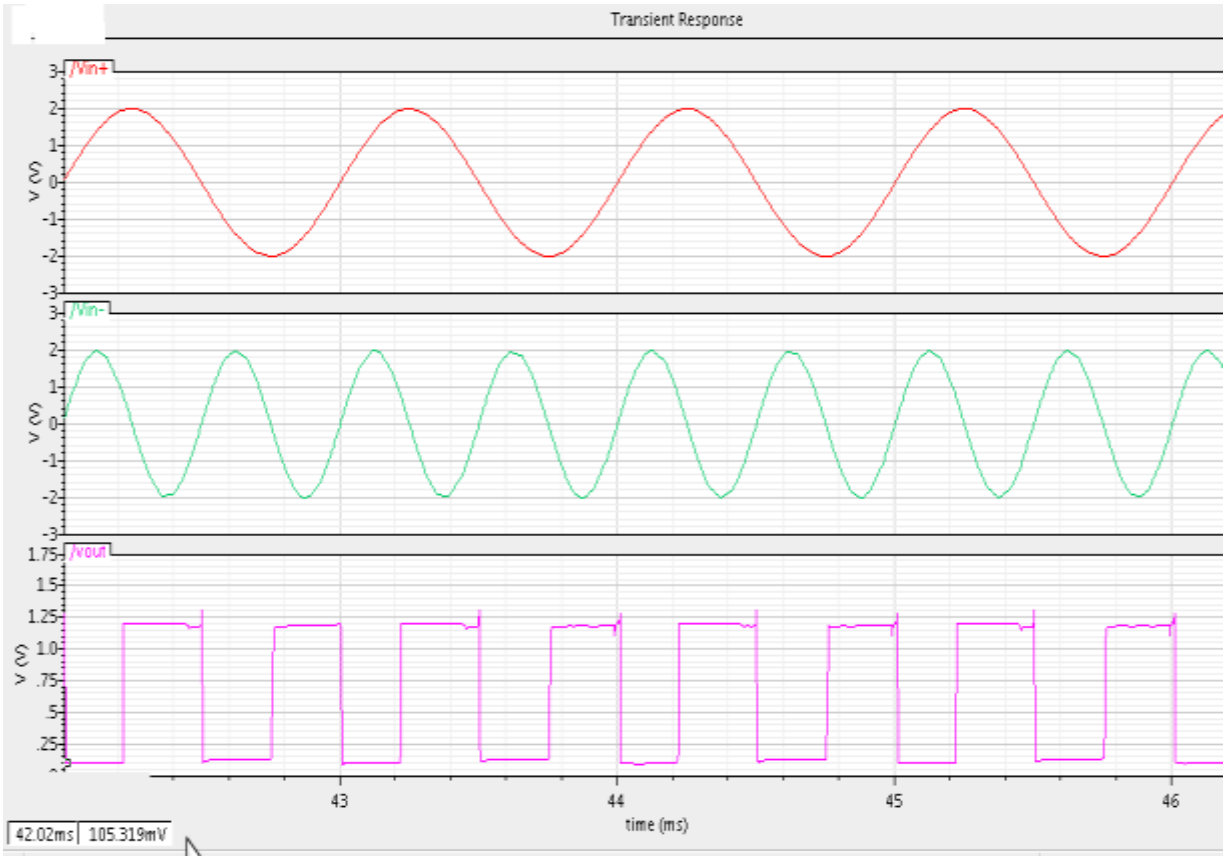


**Fig 3: Transient Analysis of CMOS comparator with Vin=1.2V**

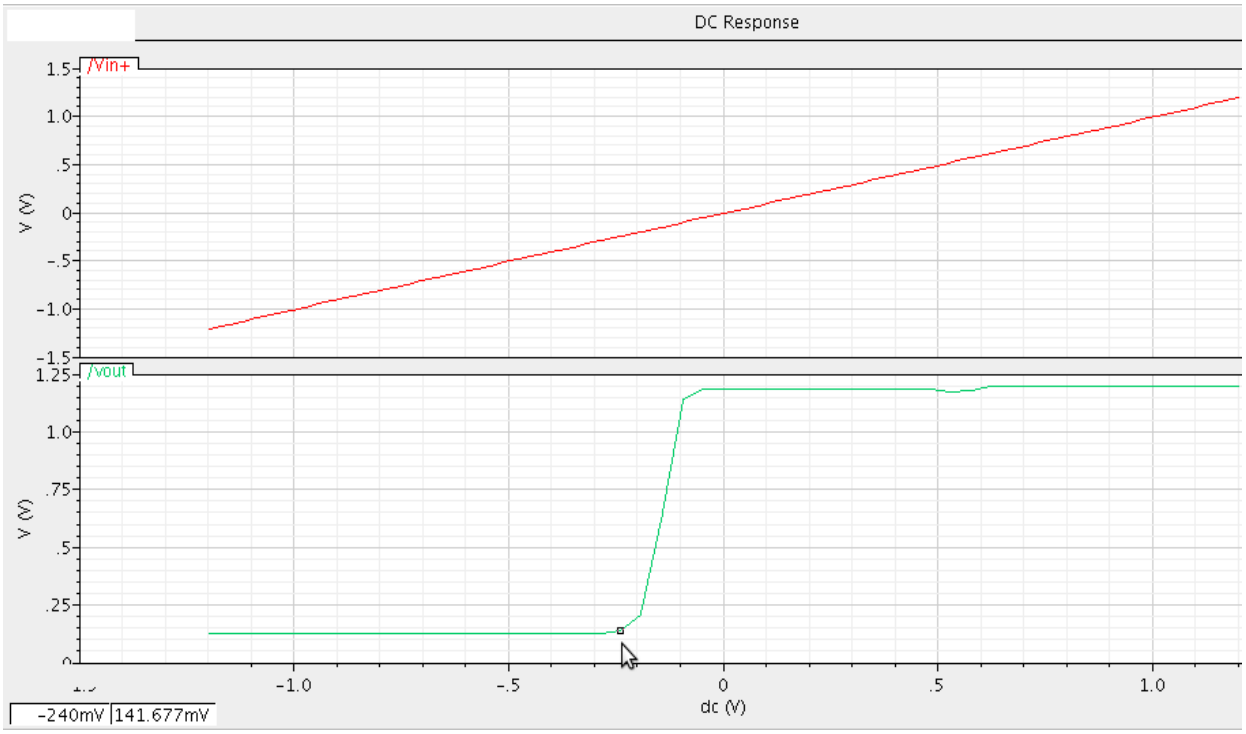


**Fig 4: Offset voltage of a comparator**

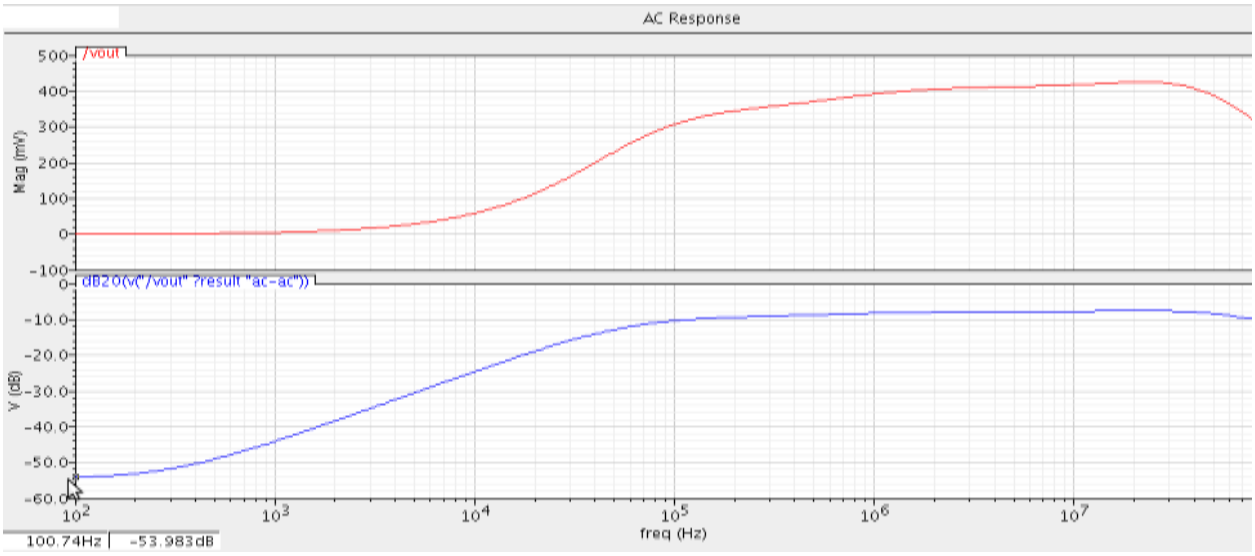


**Fig 5 : Gain of the comparator**

Next we consider the design of slew rate, rise time, fall time, power dissipation, delay, gain ,offset voltage, and area calculations in the below table

| **Parameter** | **Value** |
|---|---|
| Power supply | 1.2v |
| Power dissipation | 360 µW |
| Offset voltage | 240 mV |
| Delay | 292.3 µsec |
| Rise time | 2.727 µsec |
| Fall time | 2.727 µsec |
| Slew rate | 363.7 kV/Sec |
| Area | 180fsqm |
| Technology | 90nm |
| Clock frequency | 100MHz |
| Gain | 53.98dB |

## 5. Conclusion

In this work we proposed a high performance CMOS comparator with low offset voltage with high gain. The CMOS comparator will work in 90nm technology and results are discussed. The proposed CMOS comparator will operate at a power supply of 1.2V with offset voltage 192mV and power dissipation 1.2mW also we have carried out an output buffer stage for CMOS comparator in this stage the glitches present in the circuit are reduced. The objective has been achieved that is the proposed design of CMOS comparator as produced a low offset voltage and low power dissipation.

## 6. Future Scope

The main scope of future work in CMOS comparator is that we have to reduce the circuit area which is one of the important constraints in any VLSI design. The comparator converts analog signal to digital signal with a high sampling frequency. In future both area and time should be reduced so that an external circuit can be built which should reduce the both constraints.

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The authors equally contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

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**Conflict of Interest**

The authors have no conflicts of interest to declare that are relevant to the content of this article.