Fault Protection Considerations for MVDC Shipboard Power Systems Operating with Pulsed-Power Loads

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Abstract: - Medium Voltage Direct Current (MVDC) power distribution architectures are of immense interest for various shipboard power applications due to their advantages over classical MVAC distribution systems with respect to power quality, power density, and efficiency. However, MVDC are far away from maturity when compared to MVAC with respect to fault detection and isolation. Currently, there are no standards available for applying MVDC protection systems in shipboard applications. Furthermore, due to the absence of zero crossings in DC waveforms and unique transient fault signatures, it is challenging to design effective protection system schemes to isolate faults via conventional protection systems. This paper investigates and analyses various types of shipboard MVDC dynamic fault behaviours and signatures under different DC bus disturbances such as: bus to ground, bus to bus to ground, and impact of Pulsed-Power Load (PPL) with and without faults on a shipboard MVDC distribution system. Furthermore, a communication-based fault detection and isolation system controller that improves upon a directional ac overcurrent relay protection system is proposed offering additional protection discrimination between faults and PPLs in MVDC systems. To validate the effectiveness of the proposed protection controller, different bus current disturbances are simulated within a time-domain electromagnetic transient simulation of a shipboard power system including a PPL system operating with different ramp rate profiles, pulse widths, peak powers, and fault locations.

Key-Words: - Fault, Protection, MVDC, Pulsed-Power, Disturbance, Detection, overcurrent, relay, and isolation.

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1 Introduction

Over a century ago, alternating current power distribution systems prevailed over direct current systems and have since become the standard worldwide power generation and distribution system for terrestrial and marine applications. Back then, when it was introduced during “the war of currents”, the AC distribution system was complemented with an electromagnetic transformer. This device which enables AC voltage levels to be raised or lowered was what led to the defeat of Edison’s DC distribution system. Unfortunately, these transformers are not compatible with DC distribution systems due to the lack of natural variation in DC.

Today, thanks to advancements in technologies mainly in the power electronics field, DC distribution systems have finally found their transformers. Power electronic converters can now be used to step-up/down DC voltages just as transformers. Thus, DC systems are poised for making a comeback over historically dominant AC system. Modular MVDC power distribution systems are now being heavily considered by the US Navy as the next state-of-the-art shipboard power distribution system. This projected evolution is identified and discussed in the Naval Power and Energy Systems Technology Development Roadmap [1, 2]. MVDC presents several benefits over the traditional MVAC distribution system when considering surface vessel applications. For instance:

- The reduction or the complete elimination of shipboard bulky transformers which in return has a positive impact on the overall vessel hydrodynamic performance, vessel size, stability, weight, and compartment space.
- The absence of cabling skin effect which enable electrons to flow through the entire conductor radius.
- Decoupling the frequency between the prime mover (s) and the distribution system.
- Simpler paralleling between two asynchronous AC systems via a DC link and manipulate the output power follow in a short time.

Due to these advantages, there is a great interest in exploring MVDC microgrids today.

On the other hand, the main challenge with the MVDC system when compared to the classical MVAC system is the absence of a standard power distribution protection system. Adding to that, the implementation of power conversion modules interfacing the DC bus makes it even harder to detect and isolate faults using conventional means. As a result, to design a robust and reliable MVDC protection system, careful consideration should be given to some of the challenges imposed by the converters such as: absence of zero crossing, the generated distortion resulting from converters fast switching actions, and the natural voltage and current limiting modes responses. Current trends in MVDC protection schemes can be categorized into two groups.

- Communication-dependent protection method which depend on an exchange of information at different zones of the system via wide area communication [13-7], [15-18].
- Communication-independent techniques which rely on the local information to protect the DC system against fault currents [6], [19, 20].

To appreciate future electric MVDC ship fault dynamic behaviors, this paper investigates and analyses various types of shipboard MVDC system short-circuit faults under different DC bus disturbances including PPL activity.

Based on the shipboard MVDC fault disturbance and PPL system responses, a communication-based fault detection and isolation system controller that extends upon ac directional overcurrent relay protection system principles is developed and proposed. The controller is designed to discriminate between system dynamic short-circuit fault and bus current transient disturbances due to a PPL. To validate the effectiveness of the proposed protection controller, different bus current disturbances are studied using the PPL system at different ramp rates, pulse widths, power levels, and locations.

2 Shipboard MVDC System Under Study

The system under test is a rectifier controlled MVDC shipboard electrical distribution system derived from [1], [3] as shown in Fig. 1. The system consists of two AC gas turbine driven synchronous generators rated at 240 Hz, 45 MVA, and 13.8 kV each. This line voltage level is currently being used only on the Ford class aircraft carriers. The two machines feed the DC ring bus through two controlled 6 pulse rectifier converters. The converters convert the AC line 13.8 kV voltage to a 12 kV DC ring bus voltage. DC disconnect switches are placed at each end of each cable section along the entire distribution system to facilitate system fault isolation. The ring bus feed two constant impedance load Power Conversion Modules (PCM). These PCM can also be used to transform the ring bus voltage to electrical power needed by other loads. The DC bus also feed two Propulsion Motor Modules, and a pulsed-power load that is used to enable system pulsed-load studies. The grounding system arrangement is via a mid-point high resistance as per IEEE Standard 1709 recommendations [4]. Hence, the generator MVDC rectifier output positive and negative buses are grounded each via a 2.5 kΩ resistor. This enables the AC generator with a neutral earth grounding path. Additionally, for the system under test, a 53.36 Ω is then designed to cap the generator fault current to its winding rating limit.

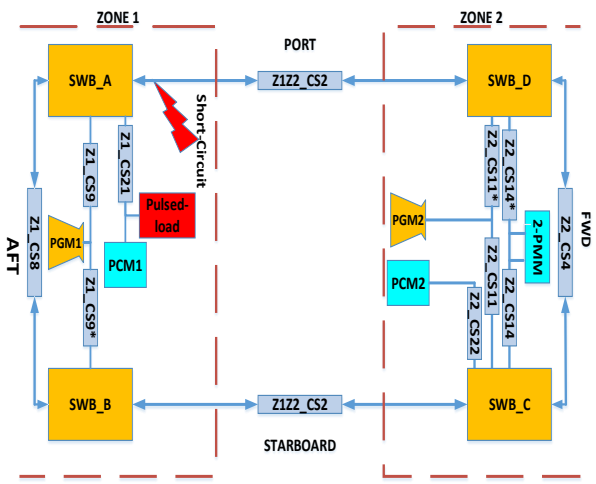

Fig. 1: A Notional MVDC Shipboard Power Distribution System

2.1 Simulation Test Results

The shipboard MVDC system described above is simulated using the MATLAB Simscape package. Different case scenarios of dynamic short-circuit fault and pulsed-power load behaviors are explored under the test system on both the AC and DC grid. Each test disturbance is triggered from a steady state operating condition.

2.1.1 (a) Pulsed-Power Load Signatures

To understand the impact of pulsed-power load on the shipboard MVDC system, a pulsed load was triggered at 0.2 seconds during operation. The system responses from the ac generation side and dc bus side are displayed in Fig. 2. The disturbance is characterized by a short grid voltage and current transient distortion. The drop in the voltage is justified by the generator's natural response to an increase in the system loading. The visible harmonic distortion is attributed to the main generator's rectification for servicing the MVDC bus. The generators momentarily tend to slow down as indicated in the RPM trend so that more torque can be picked up and react to a load increase. The spike shown on the grid current is the torque response applied to the engine rotor. The 5 ms distortion time is a result of the generator's quick response to the pulsed load. The aim of this research is not to investigate the impact of PPT on grid side, but to show:

- PPT effectively contributing short duration power injection.
- To advise future work to investigate the increased pulsed-power time constant to study system current and voltage distortion impacts and duration.

On the DC bus side, bus voltage and current disturbances are also noted in Fig. 2. This is an expected system response since no energy storage is tied into the DC bus. An interesting result is that it took the bus voltage about 0.106 seconds to stabilize while it only took the bus current 0.061 seconds. This is an unexpected discovery because it is not observed in typical shipboard power distribution systems between grid voltage and current settling time. *A* pulsed-power load disturbance on a conventional (AC) shipboard power distribution system is defined by a short bus voltage drop and a short bus current spike. Generally, the settling time difference between the disturbed bus voltage and current is not noticeable. In the proposed technique, a numerical error of about 4.5% is noted with a lagging voltage settling time. In AC systems, transformers are used to interface loads and to provide galvanic protection. On MVDC distribution systems, these transformers are replaced with power electronics. Power electronics do not provide galvanic protection, but they do have their own built in protection controls which is switching between voltage or current limiting modes. Therefore, the numerical error recorded between the bus voltage and current on the MVDC system may have been a result of:

- the thyristor switching from a voltage limiting mode to current limiting mode to try to protect the DC distribution system against the current surge.
- A slow response induced by the rectifier PI controller while waiting for the error signal.
- The system time constant $T = \frac{L}{R}$
- The grid side AVR system.

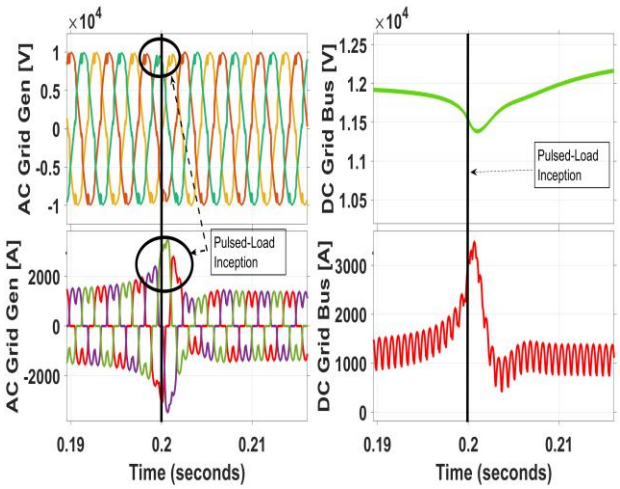

Fig. 2: Pulsed-Load Signature on the Shipboard MVDC System

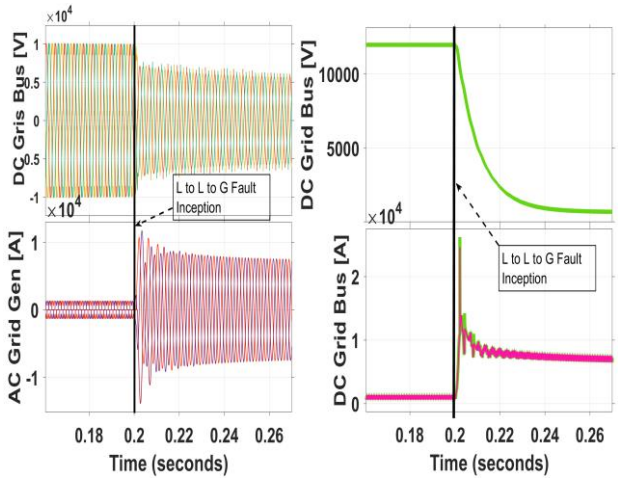

Fig. 3: DC Bus Positive and Negative Terminal to Ground Fault Signatures

2.1.2 (b) Line to Line to Ground Fault on the DC Bus

To investigate the impact of double buses to ground fault signature on the DC bus, a second simulation run was performed on the MVDC system with a bus fault triggered at 0.2 seconds shorting both positive and negative buses to ground. The grid side disturbance was defined by a drop in the AC voltage and a spike in the AC current as shown in Fig. 3.

The DC bus voltage and current system responses to the line-to-line to ground fault are also displayed in the same figure. The DC bus voltage is characterized by a voltage drop followed by an exponential decay. This fault signature can only be justified by the fact that the rectifier which was operating originally in voltage source mode went into a current-limiting mode. Power converters tend to limit fault current well below the detection threshold of protection relays which makes it difficult to detect. These are some of the operational properties of power converters which complicates the fault transient signature and protection system performance. The bus current is defined by a sudden rise, a distortion and then a decay different from the bus voltage decay. The fault signature here is a contribution of two factors: the discharge of the bus capacitor represented by the fast current peak and the inductors discharge represented by a slow decay.

2.1.3 (c) DC Bus Negative Terminal to Ground Fault

A simulation was performed with only the negative line to ground faulted to demonstrate the difference between a double line to ground fault and a line to ground fault. Interesting system responses were observed as shown in Fig. 4. On the grid side, the generator phase voltage exhibits distortions and a positive phase shift toward the positive y-axis. During normal MVDC operation conditions, DC lines balance their voltage with respect to ground depending on each line resistance. If the system is symmetrically built, each line to ground will carry half of the total voltage. Consequently, during a line to ground fault, the unfaulty line may be subject to full bus voltage. The corresponding phase current is defined by an increase on the current magnitude and a distortion on the upper part of the current waveform. The AC current waveform is also noted to be non-sinusoidal and highly asymmetrical. Converters do not decouple the AC grid from the DC grid, and in some cases due to the absence of transformers current may flow back through the generator's neutral point resistor which may cause a distortion shown in the AC current wave form in Fig. 4. A second simulation run was carried out with the positive line to ground faulted. The system response obtained on the voltage was the opposite of what was described above with the negative line to ground fault. A distorted voltage with a voltage phase shift toward the negative y-axis were noted. However, the three-phase current waveforms distortion remained the same. On the DC bus, for both simulations, a very low voltage drop is noted because line to ground fault on DC bus voltage are of relatively small magnitude. However, the DC current waveform disturbance

which resembles a three-phase half wave converter current signature could be a result of current being forced to go through only half of the converter bridge.

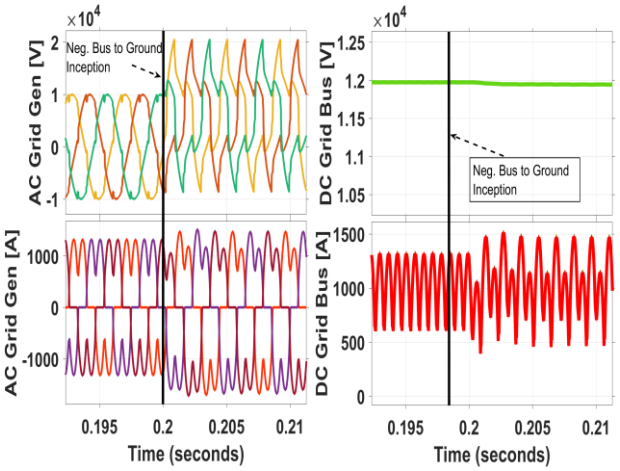

Fig. 4: Line to Ground Signature on the Shipboard MVDC System

2.1.4 (d) Line to Line Fault with Pulsed-Power Load

In this simulation, a line-to-line to ground fault and a pulsed-power load were initiated at 0.2 seconds to investigate their interactive impacts on the MVDC system. The system response that was observed were almost identical to the double line to ground fault on both the grid and DC bus side. The conclusion drawn here is, whenever a pulsed-power load and a short-circuit disturbance coexist at the same time during operation, the system response tends to mimic the short-circuit fault behavior. Therefore, conventional protection elements will have difficulty in discriminating between pulsed power load activity and genuine faults.

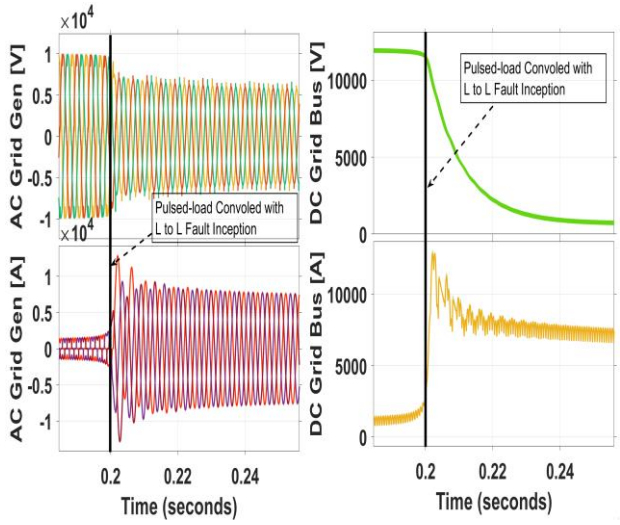

Fig. 5: Line to Line and Pulsed-Load Signatures on the Shipboard MVDC System

3 Proposed Protection System

Shipboard power systems are isolated and distributed over a short distance depending on the distribution techniques: radial, ring or zonal distribution system. Therefore, it is vital to have a secure and reliable power flow during operation especially at sea. Current trends [6-9] for instance, highlight significant research interest in MVDC distribution systems. One of the important aspects of MVDC shipboard power system design is developing a secure, robust, and reliable protection system.

As stated in [10], system protection challenges in MVDC distribution systems are mainly in fault detection, localization, and isolation. The literature has revealed five different types of fault protection techniques applicable to MVDC distribution systems. These techniques along with their differences are summarized in Table 1.

Table 1: Classification of Fault Protection Techniques

	Differential protection	Directional protection	Impedance protection	Overcurrent protection	Current derivative protection
Procedure	KCL (Current summation equal to 0)	Current reverses direction during fault	Apparent impedance drops into the tripping interval during fault	Current goes over threshold during fault	I derivative goes over threshold during fault
Networking	Dependent	Dependent	Independent	Independent	Independent
Signal Control Area	Global	Global	Local	Local	Local
Transient Sensitivity	Communication dependent	Sensitive to dynamic interactions at transients; communication dependent	Sensitive to fault impedance	Sensitive to distorted fault current waveforms	Sensitive to system noise

Thus, a communication-based fault detection, localization and isolation system controller that mimics a directional overcurrent relay protection system is developed and proposed. The controller is designed to segregate between system dynamic short-circuit fault and bus current disturbance due to a PPL. To validate the effectiveness of the proposed protection controller, different bus current disturbances are triggered using the PPL system at

different ramp time rates, pulse widths, power levels, and locations.

3.1 Overview of OCR Protection Relaying

Over Current Relay (OCR) is traditionally defined based on an electromechanical relaying protective device which operates only when the current value in a given circuit exceeds a predetermined set value, also known as the pickup, for a given amount of time. The Time-Current Characteristic Curve (TCCC) of an OCR shown in Fig.6 is used to determine the time taken by an OCR to trip a breaker for a range of over current conditions.

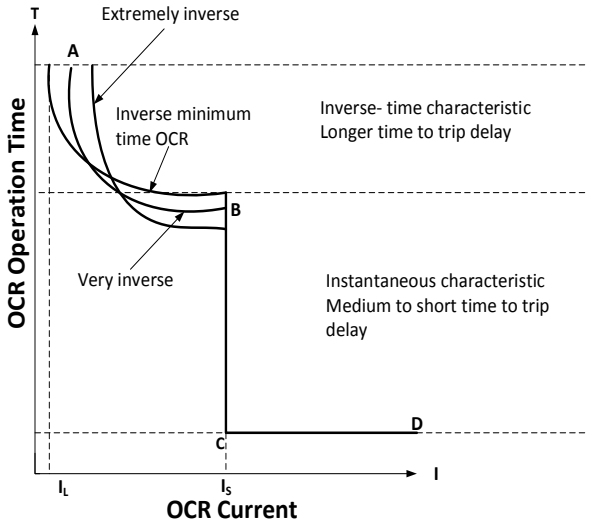

Fig. 6: Time-Current Characteristic Curve for OCR

The x-axis of the TCCC is the fault current level and the y-axis is the time taken by the relay before initiating a trip action. The A-D slope represents the OCR inverse characteristic and tends to a definite minimum operating time as the current becomes severe. The requirement for relay operation in this segment is that the more severe the short-circuit gets, the faster it should be extinguished. The reason behind that is if the overcurrent is permitted to sustain for a longer period it may cause irreversible damage to the apparatus. The B-C segment represents the OCR instantaneous characteristic, also known as the high-set. The time delay taken by the relay in sending the trip signal when operating in this segment should be shorter than the previous segment. The C-D slope represents the OCR definite minimum time instantaneous characteristic. Normally, no intentional time delay should be taken when operating in this segment, however, it may be necessary if the relay is to coordinate with downstream protection elements such as fuses.

The generic Equation of the OCR inverse-time characteristics is given as [11-13]:

$$T_{op} = \frac{TMS*\beta}{(\left(\frac{I_L}{I_S}\right)^{\alpha} - 1)} \quad (1)$$

where *TMS* (time multiplier setting) and β are two constants used to determine the characteristic of the relay, and α is the constant that determines the inverse characteristic. I_L is the load current or the instantaneous DC current and I_S the setting or pickup current. The coefficients of equation (1) determine different standard characteristics such as the normal inverse, very inverse and extremely inverse characteristics defined by the IEEE/ANSI, IEC and other standards.

Conventional AC protection relay uses fundamental frequency phasor RMS values of two AC quantities to detect the existence of a fault. These quantities are in most cases the protecting zone bus voltage and current. The signal processing in modern digital relays typically filter out all the harmonics which leads to a loss of some useful information. For instance, under an arc fault scenario, the value of the resistive component of the faulty bus impedance will increase to change the impedance angle. Since the protected bus is made up of inductance (X) and resistance (R), its fault angle depends on the relative values of the operating frequency, X and R. Consequently, under resistive conditions, a protective relay with a characteristic angle equivalent to the bus angle will underreach.

3.2 Proposed OCR Protection System Algorithm

The proposed MVDC protection controller was designed based on the system under study dynamic performances conducted in section 2. In section 2, it was demonstrated that the DC-link current signatures under PPL disturbance and a short-circuit fault are quite similar (Fig.2 & Fig.3). This problematic issue has been highlighted in [21], but until now remains unresolved in the literature. Failing to address the coexistence of a short-circuit fault and a PPL disturbance in the design of an MVDC protection system can result in an unnecessary breaker trip or

overlooking a genuine fault. Consequently, the overall shipboard MVDC system becomes unreliable. For these reasons, a suitable protection system should be sensitive to dynamic interaction during transients and to distorted fault waveforms as summarized in Table 1. In this work, under the protection system domain, a technique that detects and distinguishes these issues has been developed and tested.

3.2.1 (a) Proposed Fault Controller and Disturbances Segregation Technique

During operation of the system under test, the current flow in each power system cable section is supervised by a local communication-based protection controller. When the load current I_L is greater than or equal to the set current I_S ($I_L \geq I_S$), the section cable breaker is flagged, and the disturbance identification process is initiated. The $\left(\frac{I_L}{I_S}\right)^{\alpha}$ relation from equation (1) determines the operational time of the proposed protection controller. In the design of the protection controller, I_S is a pre-set value, and I_L is variable. I_L varies due to system disturbances from either a short-circuit fault and/or an increase in the system loading. In section 2, Fig. 3, it can be seen that the disturbance caused by a short-circuit fault on the DC grid bus current has a peak current that is almost the double of the PPL current disturbance peak shown in Fig. 5. Thus, to distinguish between the two disturbances, during operation, $\left(\frac{I_L}{I_S}\right)^{\alpha}$ component is integrated and then compared to $TMS*\beta$. As long as $\left(\frac{I_L}{I_S}\right)^{\alpha}$ integration remains under $TMS*\beta$, no action will be taken by the controller. This logic is backed up by a directional algorithm which delays the trip signal until it verifies that the DC grid bus voltage falls below some set threshold as displayed in Fig. 2. Once the DC grid bus voltage drops below the set threshold, the trip signal is released, and the corresponding breaker (s) is tripped which isolate the section cable(s). The isolated section(s) remains isolated from the rest of the distribution system as long as the fault remains. A feedback reset algorithm is set to constantly monitor the tripping logic. Whenever one or both tripping logic changes state, the reset algorithm resets the process. A close signal is automatically sent to the corresponding breaker (s) and the isolated section (s) is brought back online. The overall protection system controller flowchart is given in Fig.7 below.

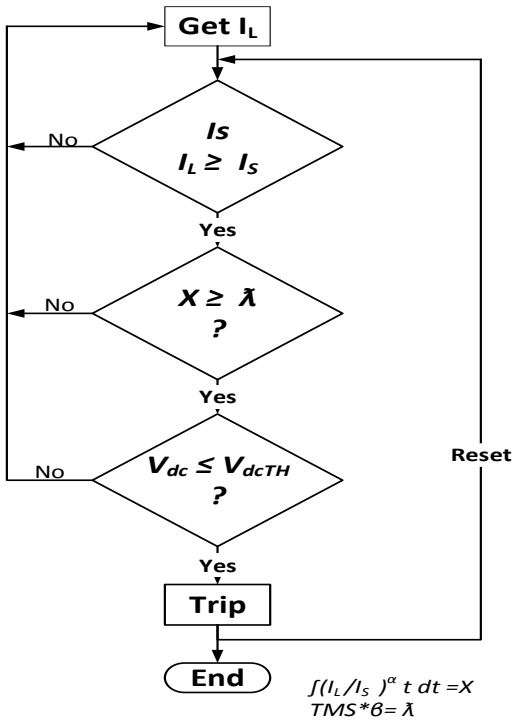

Fig.7: Proposed Protection Controller Flowchart

3.2 (b) Performance of Proposed Fault Protection Controller and Validation

The proposed controller performance and validation are studied here for different disturbance conditions on the simulated shipboard MVDC system shown in Fig. 1. The above discussed parameters used during the simulation run are as follow:

α= 0.14, β= 0.02, TMS = 8572 and I_S = 450 A

Case 1: The system was first run for 5s. At 2s after reaching steady state, a double line to ground short-circuit fault was triggered at Z1CS21 section cable (Fig.1). As shown in Fig.8(a), the fault protection controller was able to detect and isolate the faulty section within 50ms. Furthermore, the DC grid bus voltage also recovered within the same time frame. In the second simulation, an additional fault was triggered on Z2CS14 section cable 0.03s later. The protection controllers on both sections were able to detect and isolate their corresponding fault and section cable respectively. Since the second short-circuit fault was triggered before the clearance of the first fault, an additional 45ms tripping delay was noted on the second controller Fig.8(b). As a result, it took the DC grid bus voltage a longer time to recover when compared to the first simulation.

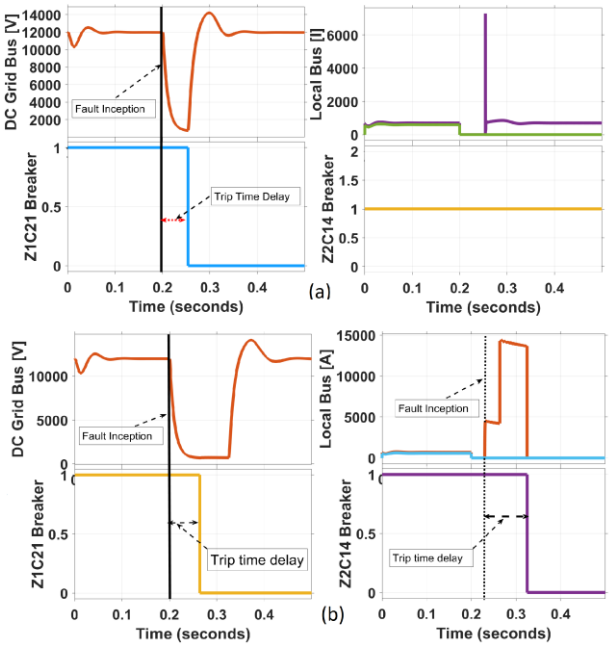

Fig.8: Proposed Protection Controller Short-circuit Response

Case 2: To validate the ability of the proposed protection controller to distinguish between short-circuit fault(s) and system bus disturbances, the following scenarios have been simulated:

- A 100 kW PPL is applied to the shipboard MVDC system at Z1CS21 section. DC grid bus voltage and current waveform disturbances have been captured and displayed in Fig.9(a). No trip response was initiated by the protection controllers.
- In the second simulation, the power level was increased from 100 kW to 500 kW and the pulsed duration from 1ms to 4ms. The DC bus voltage and current waveforms as shown in Fig.9(b) exhibit a severe disturbance. The disturbances are quite like the double Line to ground short-circuit response captured in section 2.1.2 Fig.3. However, the disturbances did not cause the proposed protection controllers to send a tripping command and thus the system was secure from a false trip.
- In the last simulation, both the 100 kW and 500 kW PPL system were triggered on the shipboard MVDC system. The DC bus voltage and current waveforms as shown in Fig.9(c) exhibited a more severe disturbance than the second simulation. However, the proposed protection system was able to discriminate between the PPL disturbance from the short-circuit fault. As a result, no tripping command was sent by the protection controllers.

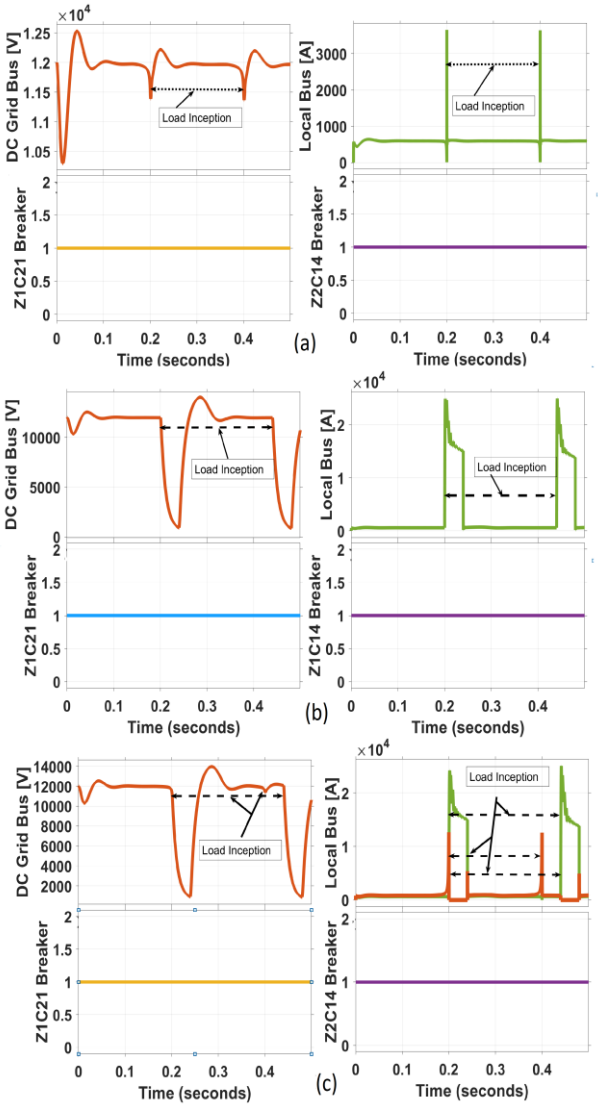

Fig.9: Impact of PPL Disturbances on the Shipboard MVDC Distribution system

4 Conclusion

This paper presents a comprehensive investigation and analysis on various types of shipboard MVDC system dynamic faults and disturbance behaviors. MVDC short-circuit faults such as positive or negative bus to ground, both positive and negative buses to ground, and Pulsed-power load (s) disturbances were the fault modes investigated along with PPL dynamics.

The main conclusions of this study are as follows:

- Based on the system responses, a novel communications-based fault protection control algorithm was designed. The proposed protection controller was designed as a solution to distinguish between system dynamic faults and transient bus disturbances such as PPL.
- The effectiveness of the novel protecting scheme to respond to short-circuit fault(s) is validated in two steps. Short-circuit faults were triggered at Z1CS21 cable section and at Z1CS21 and Z2CS14 cable sections respectively. The proposed protection system has correctly responded by detecting, localizing, and isolating the faulty section (s) in both scenarios.
- The protection scheme ability to discriminate between a short-circuit fault(s) and a PPL is also validated using PPL disturbances at different ramp time rates, pulse widths and power levels. Even though the shipboard MVDC system has experienced severe disturbances under these circumstances, the protection system trip command response remained unaffected.

The work presented in this paper offers a new approach to protecting future MVDC shipboard systems which are being heralded as the next generation of power systems for naval vessels. The results shown are encouraging in that the proposed protection system can function reliably under highly dynamic mission load profiles, offering better discrimination between future pulsed power loads and genuine faults. Future research is directed towards exploring alternative artificial and computer intelligence algorithms for expanded smart relaying applications for utility and marine power grids.

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Author Contributions:

Marounfa Djibo carried out the simulation and analysis.
Dr. Paul Moses (Expert in marine power systems and protections) and Dr. Ike Flory (Expert in power electronics, system protection and power network) have provided research guidance, analytical support, formatting and editing the paper.
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