In-Pixel CTIA & Readout Circuitry for an Active CMOS Image Sensor

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Abstract: - This work aims to design and simulate an in-pixel Capacitive Transimpedance Amplifier (CTIA) and peripheral circuitry that ensures pixel reading. Each pixel circuit is composed of four transistors using 90nm CMOS technology with a supply voltage of 1.8 V and is part of an array of pixels that make up a CMOS image sensor with peripheral circuitry. Pixel output is sent to a delta difference sampling (DDS) circuit to filter reset voltages. The Gain Margin achieved for the in-pixel CTIA is 44dB and 91dB for the Phase Margin. We also present measured pixel parameters and give a comparison with prior work. The timing and readout circuitry is also described.

Key-Words: - CMOS Image Sensor, Pixel, CTIA, Readout, Timing Circuit, DDS.

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1 Introduction

Photoluminescence-based sensors are becoming increasingly important in many environmental, biological, and health applications which need to deliver high sensitivity, high frame rate, low noise, and high dark current. Dating to the early 70s, charge-coupled devices or CCDs have served as the mainstream image sensors. Later the need for chip integration of image sensors demanded low power, low space requirements, high-speed imaging, and cost less [1][2]. Complementary metal–oxide semi-conductor (CMOS) image sensors fitting these requirements were introduced in the 1990s, which also granted lower cost, faster readout, and direct addressing of pixels, unlike CCDs which use shift registers to read out pixel data serially [3]. While CMOS image sensors were initially hindered by their higher noise levels (fixed pattern noise (FPN) was introduced) and lower sensitivity to low light levels, there have been many developments in their design to counter these limitations [4].

So, the main challenges of CMOS image sensors in low light applications are their high dark current and low signal to noise ratio (SNR) [5][6]. In this article, a new CMOS image sensor architecture is proposed to achieve high sensitivity, low noise and low dark current by using the four-transistor advanced pixel circuit feature n-well/p-sub photodiodes and a capacitive transimpedance amplifier (CTIA) for signal amplification and noise reduction. The novel design splits the amplifier with only nMOS transistors inside the pixels. Each column shares the pMOS transistors of the CTIA Additionally, Delta Double Sampling (DDS) are used as noise reduction techniques [7][8][9].

The organization of this paper is as follows: section 2 presents the architecture of the imager including the photodiode, the active pixel sensor circuit, and peripheral circuits, section 3 mainly focuses on Circuit analysis including simulation and noise analysis. And finally, section 4 gives a conclusion.

2 The architecture

2.1 General architecture

The block diagram of the complete CMOS sensor prototype is presented in Fig. 1. It contains a n rows and m columns matrix of pixels and peripheral circuits which are pixel reading circuits, sampling/holding circuits, registers to access the matrix and an analog/digital converter, this later used just for digital applications [10].

In the simplest case, only 3 transistors (3T) are needed to make a pixel, one to act as a charge reset switch, one as a column/line selector switch and the last one acts as a voltage buffer to equalize the impedances. A 3T active pixel sensor is shown in Fig. 1b where Msf is the buffer and Msel is the select switch. In this article, we focus on the design of a matrix based on a digital pixel and a circuit for reading this matrix.

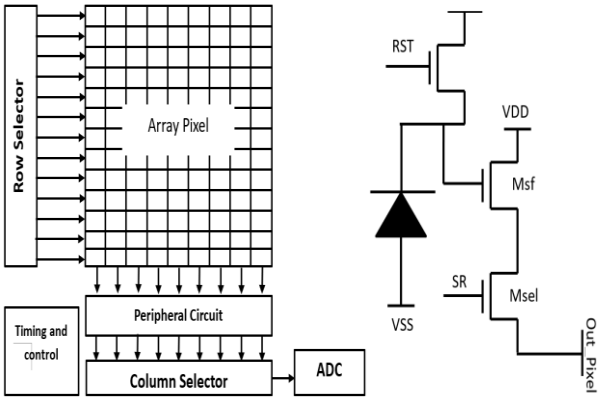

Fig. 1. a) Simplified architecture of a pixel array and surrounding circuitry. b) 3T pixel and photodiode.

2.2 In-Pixel CTIA architecture

The chip design of our architecture can be divided into three distinct parts: 1) the photodiode, 2) the capacitive transimpedance amplifier (CTIA) and 3) the peripheral circuits.

2.1.1 Photodiode

Since the photodiode is the basis of the image, it is important to note some of its characteristics. For image sensors, photodiodes are primarily used in the photoconductive (reverse-biased) mode, in which a current is generated in response to incident light. The ratio between the generated photocurrent and the power of the incident light is called spectral reactivity and is expressed in A/W. It is not easy to calculate the reactivity, especially because it depends on the wavelength due to the quantum efficiency. If the performance of the image sensor also depends on the pixel and the peripheral circuits, as well as the photodiode plays a limiting role. The material parameters control the performance of the photodiode and cannot be changed by a user [11]. There are different structures of photodiodes among them:

N+ / Psub: the simplest structure used to create a photodiode. In terms of design rules, this structure is the most compact. It is formed by creating a heavily doped region in the substrate. Due to the high doping concentration of the implant the width of the depletion region is small, and the capacitance of the junction is large. This leads to a reduction of the collection efficiency and results in a low charge-to-voltage conversion especially at long wavelengths.

n-well/p-sub: This photodiode uses lightly doped n-well diffusion to create a junction in the substrate. The lower n-well doping concentration increases the depletion width, and this decreases the junction capacitance. The larger depletion region should lead to better collection efficiency and the smaller capacitance should improve charge-to-voltage conversion. The design rules require larger minimum spacing and minimum widths for n-well versus regions. Thus, given a constant size, a pixel with an n-well photodiode will have a lower fill factor than one with a p-sub photodiode.

In an application requiring very high-resolution imaging and that the lighting is not paramount, the n+/p-sub photodiode is the most appropriate. But on the other hand, imaging in the medical domain (fluorescence imaging) Increasing the intensity of the incident light is not recommended because it leads to rapid photobleaching of the dyes. Thus, the photodiode of choice would be one with high sensitivity and low dark current the n-well/p-sub photodiode as our case. Because in terms of sensitivity, the n-well/p-sub diode is the best performing, and the signal to noise ratio was also so a lower dark current. Due to limited access to the model libraries in Cadence, the diode could not be used, but instead a current source and a parallel capacitor were used to build a photodiode, which was also suitable for the simulations. Fig. 2 below shows a circuit equivalent to a photodiode.

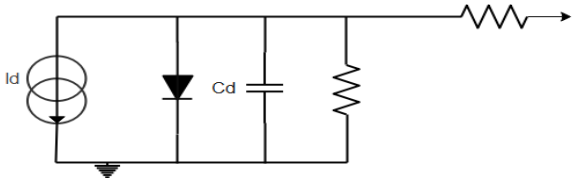

Fig. 2. Photodiode equivalent circuit includes current source, diode, a capacitor, and shunt resistor.

2.1.2 In-Pixel Capacitive Transimpedance Amplifier (CTIA)

Transimpedance amplifiers (TIAs) are used to convert a current signal to a voltage one. In photoconductive mode, inverting CTIAs are used [12][13]. TIAs present a low impedance to the photodiode and isolate it from the output voltage of the op-amp. Regarding the CTIA presented here, current integrates on the feedback capacitor in a similar fashion to an integrator op amp. They employ a 4T nMOS M1-M4 active pixel sensor with a feedback capacitor. The feedback allows the circuit to have a more stabilized bias through the photodiode, allowing a more accurate reading of the photocurrent. Their pixel circuit is a simple cascoded inverter with M5 and M6 acting as the cascode stage used to complete the CTIA. Fig. 3 displays a schematic of the pixel circuit in Cadence with respective voltage and bias sources.

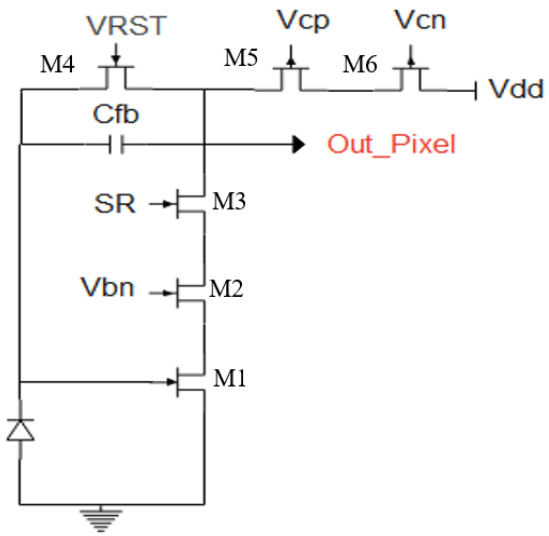

Fig. 3. In-Pixel CTIA circuit and corresponding DC voltage sources designed using Cadence.

Transistor M1 is kept in subthreshold in order to generate a gain with minimal current and M2 is biased and sized to be in saturation in order to provide a high gain. Transistor M3 serves as select switch. When row select (SR) pulse signal presents a high, M5 and M6 are shorted allowing an output path for the light generated voltage. When SR is low, pixels are floating, and the voltage measured is that generated by M5 and M6 PMOS transistors which act as a resistance. M4 serves as a reset (RST) transistor; when RST is pulsed high, M4 shorts the capacitor allowing it to discharge and thus reset its voltage prior to the next pixel integration period. Note that here the feedback capacitor is charged up towards Vdd in response to light and not down towards ground as most pixel circuits are when utilizing photodiode capacitance or Cd rather than feed-back capacitance Cfb as the integrator.

The pixel circuit here can be seen as an integrator op amp. As the capacitor in the feedback loop (Cfb) accumulates charge, the output voltage decreases to counteract the increase as a regular operational amplifier would but is then inverted thus, we see an increasing voltage while Cfb is charging during the photo integration period.

Using the input node of the CTIA, we can write:

$$I_d(s) + \left(\frac{V_{out}(s)}{G} - V_{out}(s)\right) sC_{fb} + \frac{V_{out}(s)}{G} sC_d = 0$$

We can use Kirchhoff's law to determine the theoretical value of the pixel output voltage

$$V_{out} = \frac{I_d}{C_{fb}\left(1 - \left(1 + \frac{C_d}{C_{fb}}\right)\frac{1}{G}\right)}$$

Where A is the open-loop gain. Assuming A >> Cd/Cfb >1,

$$V_{out} \approx \frac{1}{C_{fb}} \int I_d \, dt$$

This above assumption is appropriate as Cfb must be very small to allow for sufficient photo-integration. Such that the capacitance Cfb is a design parameter, unlike the capacitance Cd, which is associated with the size and type of junction of the photodiode.

2.1.2 Delta Difference Sampling

Not all pixels are reset to the same value during readout. In order to eliminate con-founding baseline values among pixels, all light-dependent pixel signals are compared and subtracted from their respective subsequent reset value. The circuit implemented to do this is called a Delta Difference Sampling circuit (DDS). It is similar to the com-monly known Correlated Double Sampling (CDS) but does not require in-pixel memory. Importantly, there is one DDS circuit per column of pixels. A sample and hold (S/H) circuit is used to implement delta difference sampling. This is shown in Fig. 4a. Fig. 4b illustrates the inside of the triangle in the S/H circuit. It is a small inverter amplifier composed of two NMOS and two PMOS transistors [14].

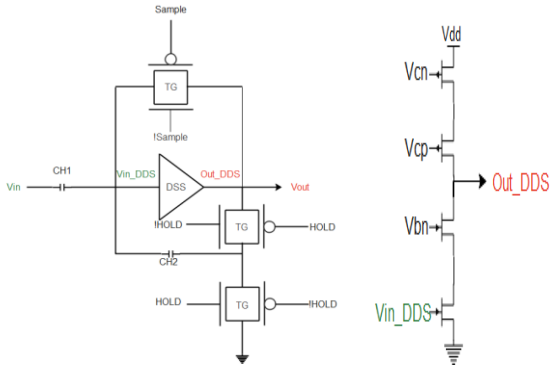

Fig. 4. (left) Delta difference sampling circuit. Top wire input is provided by Out_Pixel of Fig. 3b (right) schematic of the inside of the DDS circuit. Two NMOS and two PMOS compose a sec-ond inverting amplifier.

The floating wire coming into the S/H circuit via CH1 in Fig. 4 (left) is connected to Out-Pixel seen in Fig. 3 TG-based switches are used for the HOLD signals and sample. Sample and !HOLD are independently controlled clocks while RST and HOLD are the controlled by the same clock signal. The periods and pulse width of the clocks are shown in Table 1 while an illustration of the clock signals can be seen along with sim-ulation results in section III. TG-based switches close when a high clock pulse of 1.8V is sent into the switch. At the end of a pixel's integration period, sample (Sample) is pulsed high

(always with row select) and the total charge on CH1 and CH2 is,

$$Q_{sample}=(V_{sample}-V_{sig})*C_{H1}+V_{sample}*C_{H2}$$

Where V_{sig} is the pixel output after integration and v_{sample} is the voltage at the inversion point of the S/H amplifier. Following this stage, RST and HOLD are set ti a high, in order to measure the reset voltage of the pixel. Thus, the input of the S/H circuit may change by ΔV during the transition, therefore changing the output by GΔV. Thus, the charge on C_{H1} and C_{H2} at the end of the hold phase is,

$$Q_{HODL}=(V_{sample}+\Delta V-V_{RST})*C_{H1}+((V_{sample}+\Delta V)-(V_{sample}+G\Delta V))*C_{H2}$$

Since there is no path to ground for C_{H1} and C_{H2} to discharge $C_{H1} = C_{H2} = C$. Therefore,

$$Q_{sample}=Q_{HOLD}$$

$$2V_{sample}-V_{sig}=V_{sample}-(G-2)\Delta V-V_{RST}$$

Note that the output of the DDS circuit is Vsamp+GΔV and we can derive $V_{sig}-V_{RST}$

$$V_{sig}-V_{RST}=V_{samlpe}+(G-2)\Delta V$$

Clock	V1(V)	V2(V)	Delay(us)	Pulse width(us)	Period(ms)
Sample	0	1.8	50	50	1
!HOLD	1.8	0	0	100	1
HOLD	0	1.8	0	100	1
RST	0	1.8	0	100	1

Table 1. Clocks used in the S/H and pixel circuit.

2.1.2 Readout & Peripheral Circuitry

Controlled to read out the voltage generated after complete integration as well as the reset signal. In general, the first row of pixels in an array is selected with SR. This out-puts the light-dependent signal of all pixels to their respective column DDS circuits which samples the light-dependent signal and holds the reset signal, seen for 3 pixels in Fig. 5 The hold signal is held during the entire row readout (all columns). A column clock is therefore pulsed within each consecutive row. A diagram of the respective clock signals is shown in Fig. 6.

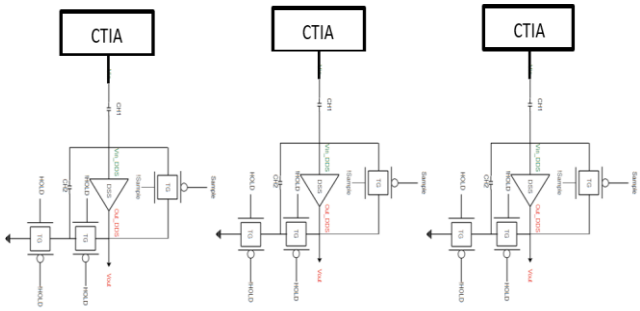

Fig. 5. Preview of CMOS pixel array including 1 row of 3 pixels.

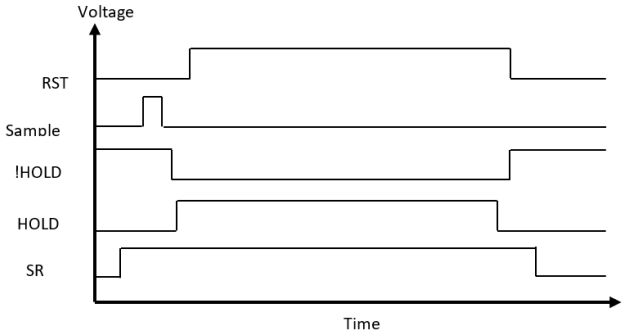

Fig. 6. A diagram of the respective clock signals.

We have 32*32 pixels, we can use a shift register with one input and 32 parallel outputs that is able to activate one input line at a time to select a single column. Two inputs will not be active at the same time thanks to the shift functions of the D flip-flops which is the basis item of the registers. Once a single output line of the shift register with 32 parallel inputs is active, it can record the pixel signal coming from that given column.

3 Simulation resullts

As indicated previously to perform the simulations we used a current source and a capacitor in parallel instead of a photodiode as shown in Fig. 2. In addition, to simu-late an output, SR must be kept high, so we used a SR without clock "SRnonclk" which presents a constant high pulse, this is used for one pixel to run the simulation. Table 2 displays the numerical values of the circuit components seen above.

3.1 In-Pixel CTIA

Transient and AC simulations were used to simulate photo-integration by the pixel. In a CTIA pixel with an ideal transimpedance amplifier (TIA), the photodiode is held at a constant voltage. In this work we use the TIA which has a single-ended cascade common-source amplifier. During the reset phase, the pixel circuit output is reset by Vrst of the TIA

input transistor. Fig. 6 shows the RST signal (Vrest) with the output of the pixel (OUT) without DDS. The output of the pixel circuit is about 420 mV to 590 mV due to the value of the feedback capacitor which is 0.1fF. In this work, we use 90nm CMOS technology which allows to limit the choice of all DC bias and transistors signals.

DC Bias Voltage		Current Source	Capacitances
Vdd=1.8V		Iac=6pA	Cd=150fF
CTIA	Vcn=1.2V	Freq=500KHz	Cfb=0.1fF
	Vcp=1V		
	Vbp=1V		
DDS	Vcn =1.2V	Idc=500fA	CH1=CH2=100fF
	Vcp=500mV		
	Vbp=700mV		

Table 2. Values used in this work, with 90nm cmos technology.

Fig. 7 shows CTIA simulation with DDS which presents a sampling signal in time varies from 0,25V to1.8V, this sampling performed thank of sampling/holding circuit.

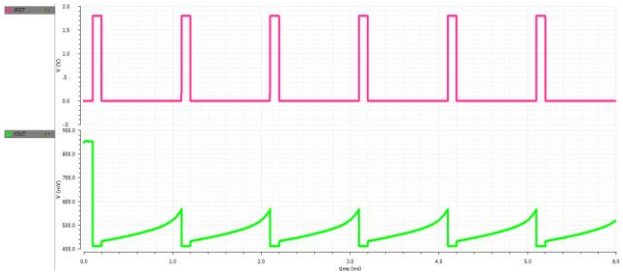

Fig. 7. Simulation of the pixel circuit without DDS with 0.1fF.

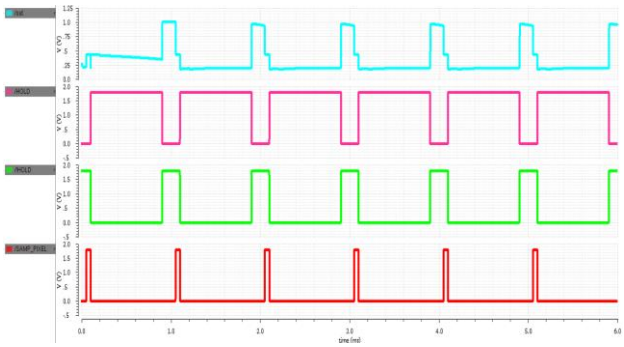

Fig. 8: Simulation of the pixel circuit with DDS.

Fig. 8 shows the stability analysis of CTIA. When the frequency is lower than f3dB = 83.7 kHz, voltage gain is arround 26.37dB. in other hand the gain-bandwidth is ap-proximate 1.79 MHz, and phase margin is 91.7-degree. The gain margin is 44.22dB with a frequency equal to 199.3MHz. According to these values, it can be no-ticed that our circuit is stable.

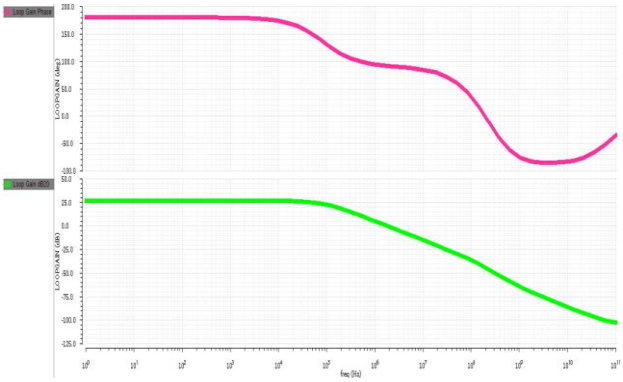

Fig. 9. AC gain margin (green signal) and phase margin (pink signal) for the in-pixel CTIA.

3.1 Noise Analysis

Transient and AC simulations were used to simulate photo-integration by the pix-On CMOS image sensors, two types of noise can be identified: temporal and spatial. The first is related to the difference between two successive samples on the same pixel under constant illumination; the sources of temporal noise are electronic shot noise where produced due to the random nature of the electrons and explains the fluctuations of the currents present on the photodiode. contribution is from the CTIA formed by M1, M2, M5 and M6 with noise from M1 dominating. It can often be overlooked. Flicker noise is a dominant source of noise for long exposure times (low light), and it can be neglected as the frequency increases in shorter exposure times. Reset noise This is thermal noise in the CMOS image sensor. Suppression depends on implementing reduction techniques in the pixel's configuration, such as active reset or flushed reset. Noise floor Is a noise that comes from the readout electronics, not including the noise generated from the photodetection. On the other hand, the spatial noise, or Fixed Pattern Noise (FPN) represents the circuit's spatial non-uniformities, and it depends on the fabrication process. Variations in the threshold voltage of the pixel's source follower are one of the main contributors to this type of noise at the pixel level. Any mismatch in the in-pixel photodiodes and feedback capacitors, and the column parallel DDS circuits will manifest as FPN. Fig. 9 shows the noise simulation.

Fig. 9 (pink) shows the noise simulation of CTIA without DDS. This analog simulation shows the output voltage noise.

The noise of the output voltage seems drop from -90V/√Hz to -140V/√Hz at fre-quency range from1 Hz to 100 MHz, which gives a variation in noise is about 50V/√Hz. So, in our work, we used DDS to eliminate this noise. Fig. 9 (red) shows the simulation of the noise of the output voltage of CTIA with DDS which drop from 710.5nV/√Hz to 147.42nV/√Hz, which is almost 563.1nV/√Hz variation in noise.
In-Pixel CTIA is implemented in 90 nm CMOS technology. Fig. 10 shows the lay-out of the design presented in this paper. The layout area of this work is 100.28um^2. The capacity of the photodiode occupies 42.1% of the total layout area (Fill Factor).

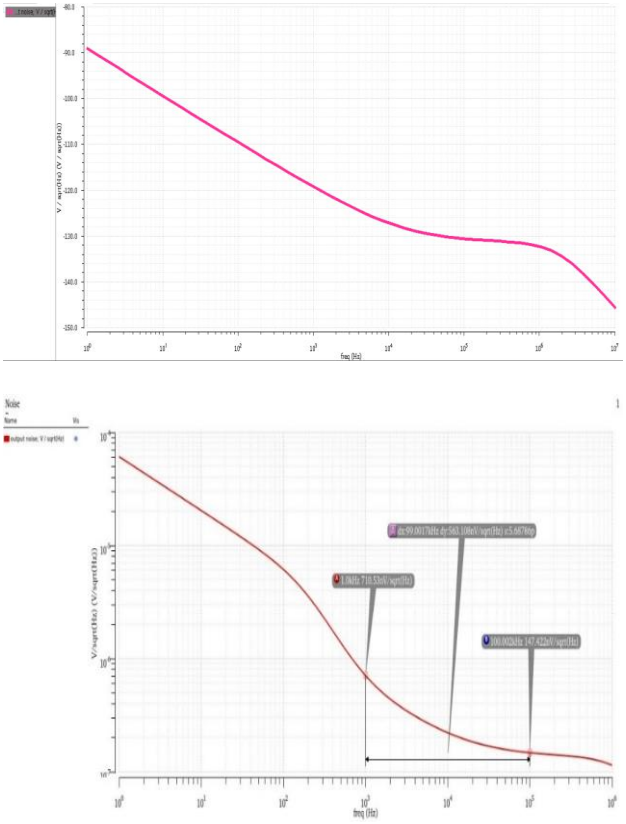

Fig. 10. Noise simulation of CTIA without DDS (pink), without DDS (red).

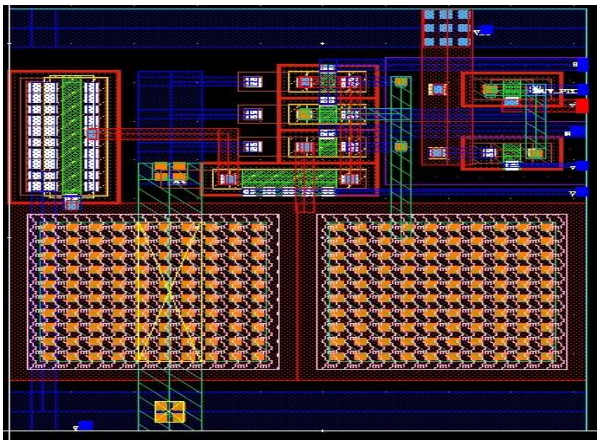

Fig. 11. Layout of the in pixel CTIA.

	[13]	[14]	This work
Chip resolution	3000*3000	2560*3072	32*32
Pixel size	6.5um*6.5um	6.5um*6.5um	9.2um*10um
CMOS technology	0.11um	180nm	90nm
FD capacity	19.6fF	19.6fF	0.1fF
Pixel type	4T	5T	4T
Fill factor	67.4%	100%	42%

Table 3. Performance comparison between a previous and this works

4 Conclusion

This work describes and replicates an in-pixel capacitive transimpedance amplifier as well as a delta-difference sampling circuit and the corresponding peripheral timing circuitry. Although not covered here, analyzing the 1/f and fixed pattern noise present in any image sensor is vital to its realization. FPN firmly presents itself when there exists pixel- level mismatches in the feedback capacitance and column-level mismatches in the S/H circuit capacitor ratio C_{H1}/C_{H2}. Noise analysis shows that is almost negligible.

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