A Novel low power 2-D to 3-D Array Priority Encoder using Split-Logic technique for Data Path Applications

D. S. SHYLU SAM[1]*, P. SAM PAUL[2], JENNIFER ELIZAH[3], NITHYASRI[4], SNEHITHA[5], AKANSHA SINGH[6], VIJENDRA[7]

[1,3,4,5,6]ECE Department,Karunya Institute of Technology & Sciences, Coimbatore, INDIA
[2]Mechanical Department, Karunya Institute of Technology & Sciences, Coimbatore, INDIA
[7]CG Coreel Technologies Pvt. Ltd., Bangalore, INDIA

Abstract: - In this work, an ascendable low power 64-bit priority encoder is designed using a two-directional array to three-directional array conversion, and Split-logic technique and 6-bit is obtained as the output. By using this method, the high performance priority encoder can be achieved. In the conventional priority encoder, a single bit is set as an input, but for a priority encoder with 3-Darray, every input are specified in the matrix form. The I-bit input file is split hooked on M × N bits, similar to 2-D Matrix. In priority encoder with 3-Darray, three directional output comes out, unlike traditional priority encoder, where the output is received from one direction. The development can be achieved by implementing the two-directional array to three-directional array technique. Simulation results show that the proposed 2-D and 3-D priority encoder consumes 0.087039mW and 0.184014mW which is less when compared with the conventional priority encoder. The priority encoders are simulated and synthesized using VHDL in Xilinx Vivado version 2019.2 and the Oasys synthesis tool.

Key-Words: - Priority Encoder, split-based technique, low power, Synthesis, HDL,Netlist

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1 Introduction

A Priority encoder is an algorithm or a circuit that compresses a larger number of binary inputs into a smaller number of outputs[1-2] The inputs to the encoder are 2^nbits inputs and produces n-bit output. The output of the priority encoder number starts from zero to the most significant input bit. The performance of the priority encoder increases rapidly, especially for processing a high number of input bits[3-4]. The outputs address can be achieved as binary arrangement, from where parallel data can be regained suitably.

As the computer system and technology became faster, the need for transportable electronics encourages the progress of the power consumption in the Priority encoder structure[5-6]. Therefore, the performance of a priority encoder is increasing speedily since input size is also increased by any numbers of bits[7].

Therefore, certain principles suggest covering the 2-D to 3-D conversion depending on priority encoder, to construct an ascendable high-performance Priority encoder. It mainly emphasizes a methodology to build 2^n input bit that is 64-bit and larger sized Priority encoder can be designed based on this technique.

2 Problem Formulation

To decrease the consumption of power in electronic devices, keyboard applications, robotic arm control, ship movement ,etc. several methods were suggested in the literature. In parallel priority look ahead 64-bit priority encoder, there are 64 sets of inputs that are distributed as 8 sets, that is 8X8=64. The 64 sets are given as input to eight OR gates that are aligned parallel to each other and also 8:1 multiplexer which gives 8-bit output. The outputs of the OR gate and the multiplexer is given as input to the 8:3 priority encoder, and the outputs of the priority encoder is then combined to give out 6-bit output, using this method power consumption can be reduced. This architecture is used to decrease the Propagation delay and it is used for low and high priority estimation with a flexible structure. The low power and high speed achieved by the priority encoder design when compared to the power consumed by the domino dynamic [8-9] circuit is

more at unwanted redundant power switching at various dynamic power nodes.

In this paper [10-11] multi-level look-ahead technique is implemented to reduce the consumption of power and also to increase the speed of the circuit. The full parallel priority encoder is designed as it would upsurge the performance of the circuit. One of the other approaches is GDI [12-13] which is also used in the reduction of power consumption. The performance of the circuit depends upon the factors such as delay and power; these factors are decreased during the optimization of the circuit done by executing the latest circuit that includes priority look-ahead parallel architecture [14-15].

The copious quantity of bits is distributed from which only the needed bits are sent as inputs. For example, 1,024 bits are separated into eight 128 bits and procedures. Similarly, the data that is the form of the matrix are stocked in recollection and computed in this work. In multi-match, all the inputs given to the priority encoder, that is 64 bits are then craved up into eight sets each containing 8-bits. As per the split-logic technique, these groups are given as input to the 8-input OR gates. Therefore, eight OR gates deposited parallel to each other, generating eight-bit output. In the architecture of a 64-input priority encoder, the whole of 64 inputs is distributed as smaller sets and every set contains eight bits. So, OR gates with eight inputs are aligned in parallel to each other and gives 8 single-bit outputs. These outputs are given as input to the eight into three priority encoders, causing three outputs. An eight-input MUX circuit is also used to take inputs that are applied for OR gates and these 8 outputs are the inputs to eight into three priority encoders, which further gives out three outputs. Therefore, combining the priority encoders gives six-bit outputs.

3 Problem Solution

3.1 2-D array Priority Encoder

In the 64:6 2-D array priority encoder, there are 64 inputs. The 64 bits are given to the input of 8:1 OR gates as OR0, OR1, up to OR7, in such a way the gates are parallel to each other generating 8- bit outputs. The input of the 8-input priority encoder is derived from the output of 8:1input OR gates and generates 3-bit output. The 64 bits' inputs are also given to the 8-8:1 multiplexer and give eight 1-bit of output, which is further sent to the priority encoder with 8 inputs and 3 outputs. The MUX takes the selection lines from the output of the 8-input OR gate. By combining both the priority encoder of 3-bit outputs, the final output with 6-bits is generated. Fig. 1 shows the circuit diagram of the 2-D array priority encoder.

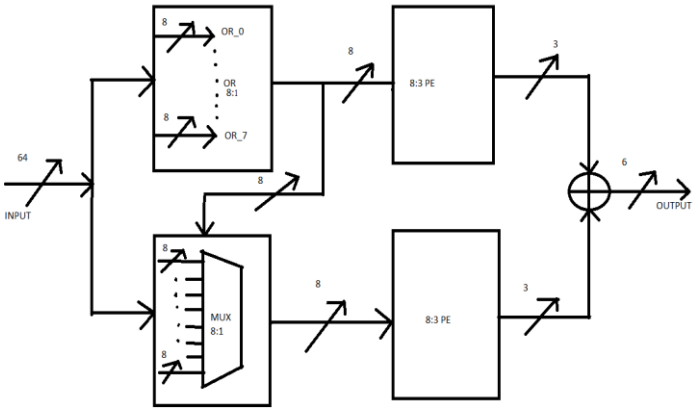


Fig. 1: Circuit of 2-D array priority encoder 64:6

Table 1. Truth Table of 16X4 Priority Encoder

Inputs																Outputs			
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Q3**	**Q2**	**Q1**	**Q0**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	x	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	x	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	x	x	x	x	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	x	x	x	x	x	0	1	0	1
0	0	0	0	0	0	0	0	0	1	x	x	x	x	x	x	0	1	1	0
0	0	0	0	0	0	0	0	1	x	x	x	x	x	x	x	0	1	1	1
0	0	0	0	0	0	0	1	x	x	x	x	x	x	x	x	1	0	0	0
0	0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	1	0	0	1
0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	1	0	1	0
0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	1	0	1	1
0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	1	1	0	0
0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	0	1
0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	0
1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1

3.2 3-D Array Architecture

The 64:6 3-D priority encoder has different sub-blocks, that contain OR gates, Priority encoders, and multiplexers. 64 inputs are given and these 64 inputs are divided into 4-bit as 16 groups, where each group consists of a total of 16 x 4 = 64-bits. OR_A block contains 16-four input OR gates, parallel to each other, giving out 16 single bit outputs where each OR gates consists of 4-bit input and generates one single output. The sixteen single- bit output coming from the OR_A block is given to

OR_B and PE_B blocks. PE_A block consists of 16 priority encoders as 4:2, and are placed corresponding to one another. The output of PE_A is 32-bit which is given as input to MUX_B. OR_B block which takes input from OR_A, consists of 16inputs placed in parallel with 4-bit to each OR gate and gives out 4 single bit outputs. And this four-bit output is given as input to 4:2 priority encoder and the output of this PE 4:2 is given as selection lines to MUX_A, MUX_B.

$$x = a_0 + a_1 + a_2 + a_3 + a_4 + a_5 + a_6 + a_7 \quad (1)$$

$$y = D_0 S_{0bar} S_{1bar} S2_{bar} + D_1 S_{0bar} S_{1bar} S_2 + D_2 S_{0bar} S_1 S_{2bar} + D_3 S_{0bar} S_1 S_2 + D_4 S_0 S_{1bar} S_{2bar} + D_5 S_0 S_{1bar} S_2 + D_6 S_0 S_1 S_{2bar} + D_7 S_0 S_1 S_2 \quad (2)$$

$$Q_{0Top} = \sum(x_{6bar} + x_{fourbar} x_{2bar} x_1 + x_{4bar} x_3 x_5) + x_7 \quad (3)$$

$$Q_{1Top} = \sum(x_{5bar} x_{4bar} (x_{two} + x_{three}) + x_6 + x_7 \quad (4)$$

$$Q_{2Top} = \sum(x_4 + x_5 + x_6 + x_6) \quad (5)$$

$$Q_{0Bottom} = \sum(y_{6bar} + y_{fourbar} y_{2bar} y_1 + y_{4bar} y_3 y_5) + y_7 \quad (6)$$

$$Q_{1Bottom} = \sum(y_{5bar} y_{4bar} (y_{two} + x y_{three}) + y_6 + y_7 \quad (7)$$

$$Q_{2Bottom} = \sum(y_4 + y_5 + y_6 + y_7) \quad (8)$$

$$Output = Q_{top} + Q_{Bottom} \quad (9)$$

The input of PE_B block which also takes inputs from output of OR_A, consists of 4 priority encoders as 4:2 and are placed corresponding to each other and develops eight-bit output, which is given as input to MUX_A.MUX_A consists of two 2:1mux circuits and generates 2bit output. MUX_B consists of two 8:1 MUX circuits and generates 2bit output. The output of 4:2 PE, MUX_A ,and MUX_B are combined to get the final output. Fig.2 shows the circuit diagram of the 3-D priority encoder.

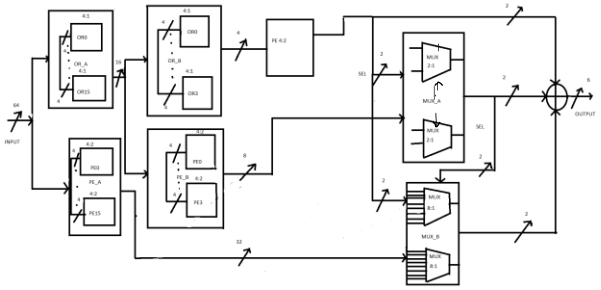


Fig. 2: Shows the circuit diagram of the 3-D priority encoder.

The internal design of the 4:1 MUX circuit is shown in Fig.3. The design generates two outputs and has six 2:1 MUX and has two selection lines. The inputs given to four 2X1 multiplexer is given as the inputs to 4X1 multiplexer. The output of the 2X1 multiplexer is given as inputs to two 2X1 multiplexer and the 2X1 multiplexer (q5) selects the inputs from q4 and provide the output as q2 and q3.

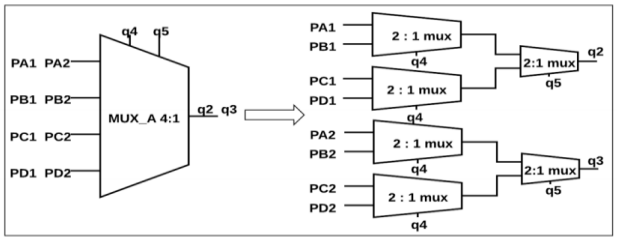


Fig. 3: Internal circuit of 4:1 MUX[2]

The internal circuit 16:1 MUX design is shown in Fig.4. The design generates two outputs has four 2:1 MUX and two 2:1 MUX and has two selection lines. The internal circuit of multiplexer and is used to select from the multiple inputs to a single input.

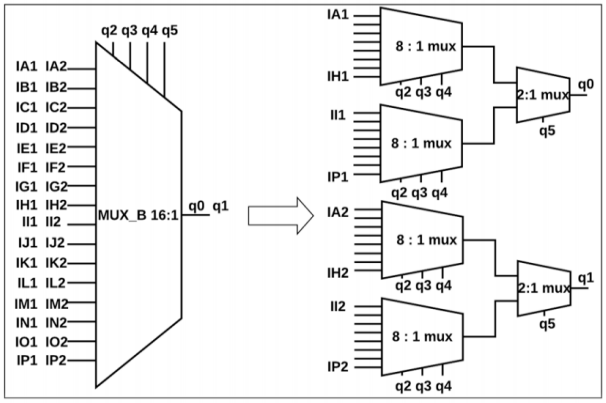


Fig. 4: Internal circuit of 16:1 MUX[2]

Power consumption is one of the essential factors in modern electronics [16-21]. But the expected power cannot be achieved due to the supply voltage, Capacitance, and input operating frequency. As the power consumption is affected by leakage current and other factors it is necessary to reduce the power consumption. The Priority encoder uses priority stage at each input. When there are multiple inputs priority encoder comes into picture and selects the high priority input and all other low priority inputs will be neglected. Hence power consumption is important in 64-bit priority encoder when used for data path applications.

4. Results and Discussion

The various logics are splitted and integrated to realize the 2-D and 3-D priority encoder using the Split-logic technique. The input of the 8-input priority encoder is derived from the output of 8:1input OR gates and generates 3-bit output. The 64 bits inputs are also given to the 8-8:1 multiplexer and give eight 1-bit of output, which is further sent to the priority encoder with 8 inputs and 3 outputs. The MUX takes the selection lines from the output of the 8-input OR gate. By combining both the priority encoder of 3-bit outputs, the final output with 6-bits is generated. The 64:6 3-D priority encoder has different sub-blocks, that contain OR gates, Priority encoders, and multiplexers. 64 inputs are given and these 64 inputs are divided into 4-bit as 16 groups, where each group consists of a total of 16 x 4 = 64-bits. The Simulation results are obtained using the Xilinx Vivado tool and synthesis reports are obtained using the Oasys synthesis tool. The power obtained from the designed priority encoder is very less when compared with the conventional priority encoder. Fig. 5,6 shows the schematic of

block design of 2-D array using Oays synthesis tool and Xilinx Vivado tool.

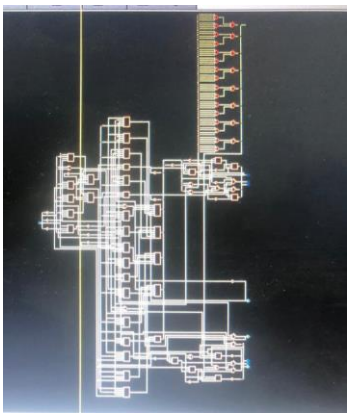


Fig. 5: Block design of 2-D array 64:6 using Oasys synthesis tool

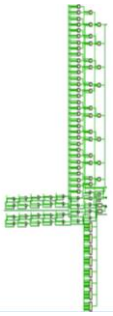


Fig. 6: Block design of 2-D array 64:6

Fig. 7 shows the waveform of the 2-D array priority encoder. The output waveform is verified as per the truth table of the priority encoder. The main advantage of this type of priority encoder is used for complex data path elements. Fig. 8 shows the netlist generated for the 2-D array encoder.

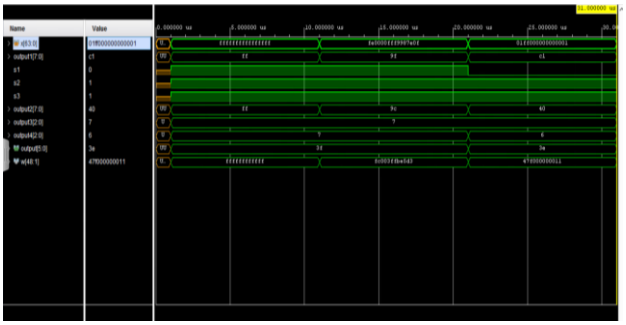


Fig. 7: Waveform of 2-D array 64:6 encoder.

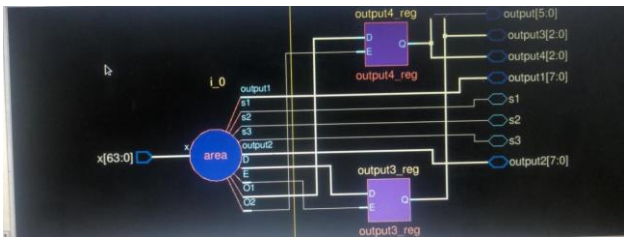


Fig. 8: Netlist generated for 2-D array encoder.

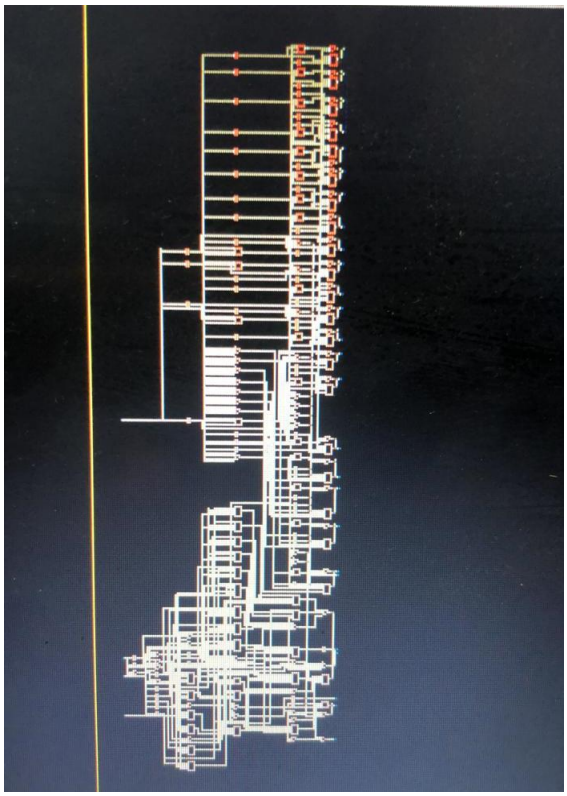


Fig. 9: Block diagram of 3-D array 64:6 using Oasys synthesis tool

Fig. 9,10 shows the block diagram of the 3-D array priority encoder. All the sub-blocks including Priority encoder, OR gate, and Multiplexer are integrated to realize the 3-D array priority encoder.

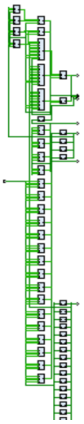


Fig. 10: Block design of 3-D array 64:6encoder

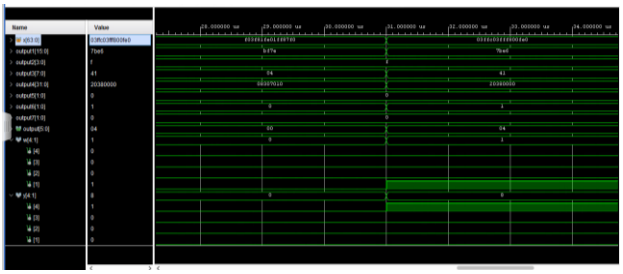


Fig. 11: Waveform of 3-D array 64:6 encoder

Fig. 11 shows the waveform of the 3-D array priority encoder. The output of the 3-D priority

encoder is verified as per the truth table. Fig. 12 shows the power analysis of the 2-D priority encoder using the Oasys synthesis tool. The total power consumption obtained by the 2-D priority encoder is 0.87039mW.

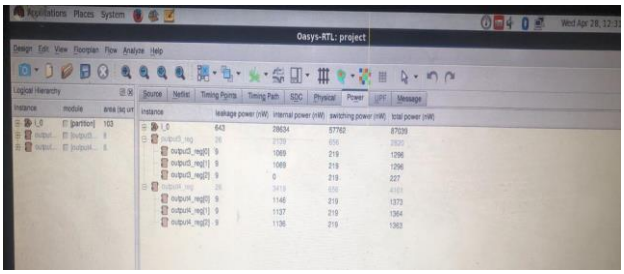


Fig. 12: Power analysis of 2-D using Oasys synthesis tool.

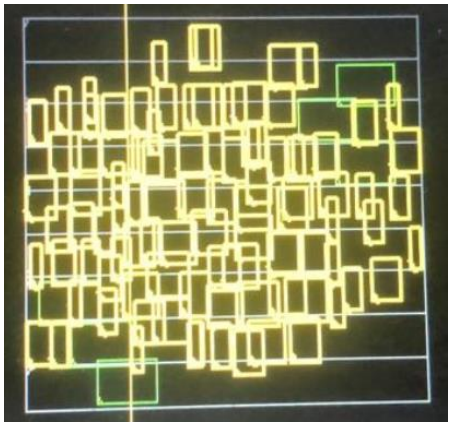


Fig. 13: Physical Verification of 2-D priority encoder

Fig. 13 shows the physical verification of the priority encoder. It shows the interconnected sub-blocks to realize the 2-D priority encoder. Fig. 14 shows the physical verification of the 2-D priority encoder with all the internal blocks.

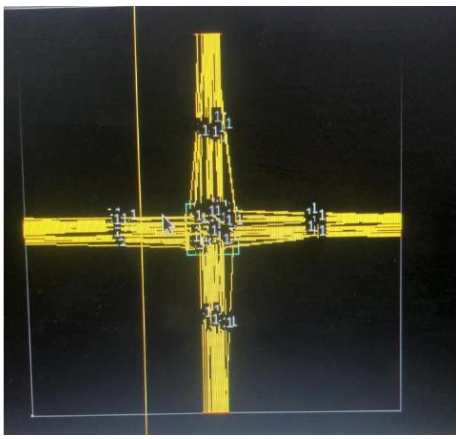
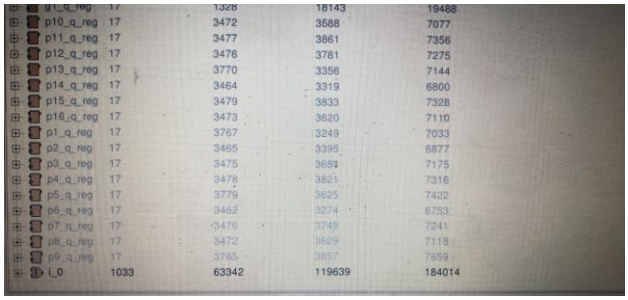


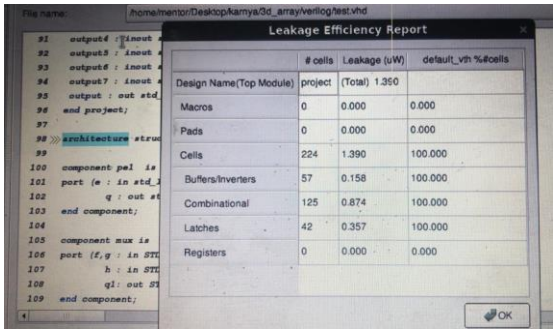
Fig. 14: Physical verification with all the logic sub-blocks.



p10_q_reg	17	3472	3588	7077
p11_q_reg	17	3477	3861	7356
p12_q_reg	17	3476	3781	7275
p13_q_reg	17	3770	3356	7144
p14_q_reg	17	3464	3319	6800
p15_q_reg	17	3479	3833	7328
p16_q_reg	17	3473	3620	7110
p1_q_reg	17	3767	3249	7033
p2_q_reg	17	3465	3395	6877
p3_q_reg	17	3475	3685	7175
p4_q_reg	17	3478	3821	7316
p5_q_reg	17	3779	3625	7422
p6_q_reg	17	3462	3274	6753
p7_q_reg	17	3476	3749	7241
p8_q_reg	17	3472	3629	7118
p9_q_reg	17	3785	3857	7659
i_0	1033	63342	119639	184014

Fig. 15: Power analysis of 3-D array using Oasys Synthesis tool.

Fig. 15 shows the power analysis of the 3-D array using the Oasys synthesis tool. The power obtained for the 3-D priority encoder is 0.184014mW.



Design Name(Top Module)	# cells project	Leakage (uW) (Total) 1.390	default_vth %#cells
Macros	0	0.000	0.000
Pads	0	0.000	0.000
Cells	224	1.390	100.000
Buffers/Inverters	57	0.158	100.000
Combinational	125	0.874	100.000
Latches	42	0.357	100.000
Registers	0	0.000	0.000

Fig. 16: Leakage efficient report

The leakage power obtained for the 3-D priority encoder is 1.390µW. Fig. 16 shows the leakage efficient report. The leakage power of Cells is 1.390µW. The leakage power reported for Buffers/Inverters is 0.158µW. The leakage power for the combinational circuit is 0.357 µW. The leakage power of the Latches reported from the synthesis report is 0.357 µW. Fig.17 shows the total cell usage report for 3-D priority encoder. In this report the total area (sqµm) is displayed for all the combinational logic. As the power consumption of priority encoder is one of the important factor the leakage power for all combinational logic is given in the report.

Cell Usage Report

Cell	Family	Type	Data	Count	Area (squm)	Total (squm)	Leakage (nw)	Total Leakage(nw)	Library
OR4_X1	OR4_X1	comb	Both	6	1.6	9.6	5.73	34.682	NangateOpenCellLibrary
OR3_X1	OR3_X1	comb	Both	2	1.3	2.7	4.959	9.919	NangateOpenCellLibrary
OAI33_X1	OAI33_X1	comb	Both	1	1.9	1.9	13.242	13.242	NangateOpenCellLibrary
OAI22_X1	OAI22_X1	comb	Both	4	1.3	5.3	8.593	34.372	NangateOpenCellLibrary
OAI221_X1	OAI221_X1	comb	Both	6	1.6	9.6	8.801	52.806	NangateOpenCellLibrary
OAI21_X1	OAI21_X1	comb	Both	1	1.1	1.1	5.333	5.333	NangateOpenCellLibrary
OAI211_X1	OAI211_X1	comb	Both	1	1.3	1.3	5.475	5.475	NangateOpenCellLibrary
NOR4_X1	NOR4_X1	comb	Both	10	1.3	13.3	9.237	92.373	NangateOpenCellLibrary
NOR3_X1	NOR3_X1	comb	Both	3	1.1	3.2	7.124	21.373	NangateOpenCellLibrary
NOR2_X1	NOR2_X1	comb	Both	24	0.8	19.2	5.012	120.296	NangateOpenCellLibrary
NAND4_X1	NAND4_X1	comb	Both	2	1.3	2.7	4.8	9.601	NangateOpenCellLibrary
NAND3_X1	NAND3_X1	comb	Both	6	1.1	6.4	4.535	27.029	NangateOpenCellLibrary
NAND2_X1	NAND2_X1	comb	Both	6	0.8	4.8	3.931	23.587	NangateOpenCellLibrary
INV_X1	INV_X1	comb	Both	57	0.5	30.3	2.775	158.201	NangateOpenCellLibrary

Fig. 17 The total cell usage report for 3-D priority encoder.

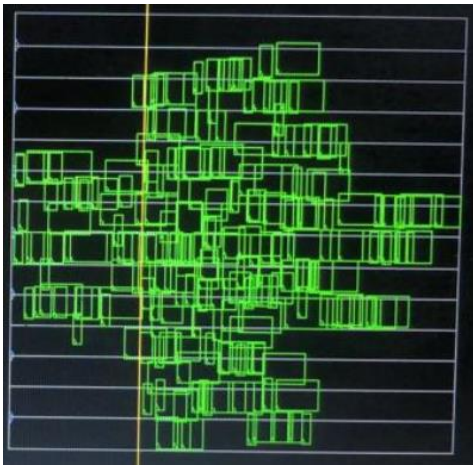


Fig. 18 Physical Verification of 3-D array priority encoder.

Fig.18 shows the Physical Verification of the 3-D array priority encoder. Thus the simulation and synthesis of 2-D and 3-D priority encoder are done and verified. Synthesis results show that the designed priority encoder consumes less power when compared with the existing priority encoders. The designed priority encoder can be used for complex data path elements including adders, multipliers, and Arithmetic Logic Units. Table 1 shows the comparison result of priority encoders with existing work.

Table 1. Comparison result with existing work

Reported Works	**Total Power(mW)**
2D-array 64:6[2]	0.3480
3D-array 64:6[1]	0.2648
Proposed 2D-array 64:6	0.087039
Proposed 3D-array 64:6	0.184014

5. Conclusion

The architectures of both the circuits are used for data-path applications and high-speed FLASH ADCs. Simulation results of two dimensional and three-dimensional array priority encoders consume low power consumption. This low power is achieved by using the split-logic technique. The priority encoder with 2 Directional-array consumes 0.87039 mW and that of priority encoder 3 Directional-array consumes 0.184014 mW. Thus, the power analysis is done and the entire design is simulated and synthesized. Simulation results show that the performance of the proposed priority encoder is high when compared with the conventional encoders. Hence the proposed encoder can be used for data–path applications.

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