Design of Self-Adaptive Weighted Neuron model using Floating Gate Technology

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Abstract: The paper presents an analog circuit solution for implementing models of synapses with short-term adaption, derives an analytical solution (Floating gate charge as weights) for spiking input signals, and presents simulation results using a 45nm CMOS process using floating gate technology. The circuit is suitable for integration in large arrays of integrate-and-fire neurons and thus, can be used for evaluating computational roles of short-term adaption at the network level. Proposed floating gate p channel MOSFET (FGPMOS) can self-adapt, learn and store data with help of external voltages highly precise non-volatile and stable programming of weights (training) after fabrication of circuit have been performed. On application of feedback in the circuit, short-term self-adaption with spiking input signal has been observed. The model can also demonstrate homeostatic intrinsic plasticity, spike-based algorithms, and LMS algorithms. The model has a 4.5μV/℃ temperature coefficient, 0.675μW power consumption, and consumes a chip area of about 130×90 nm^2. The model is compact, low power, and stable. The proposed circuit has been applied to design a cell membrane (bio-sensor CMOS-based circuit) depicting the effect of Sodium (N_A) and Potassium (K) on synaptic action. With the help of the Na and K feedback circuit, effects of polarization and depolarization on synapse output have been demonstrated and thus depict spike-timing-dependent plasticity. The work can be extended to design a complete neural architecture, an array of such complete neural cells, in turn, can design devices for assistive technology or human-like machines.

Keywords: Artificial intelligence, Cognitive abilities, Floating gate technology, Neuron, Neuromorphic circuits, silicon neurons, Biomolecular sensor
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List of Abbreviations

IOT	Internet of things
SiNs	Silicon neurons
NC	Neuromorphic circuits
STDP	Spike timing-dependent plasticity
LMS	Least mean square
ADALINE	Adaptive Linear Combiner
SP	Structural-Plasticity
VLSI	Very-large-scale integration
FG	Floating Gate
PTM	Predictive technology model
CMOS	Complementary metal-oxide-semiconductor

1. Introduction

For more than two decades, the brain and its capability of information processing principles have been a standard in building artificial intelligence (AI). AI-based algorithms allow recognition tasks and can be implemented with the help of very large-scale integration (VLSI) technology. The field of integrating brain computation-based algorithms with technology is referred to as "Neuromorphic engineering" (NE). The term 'Neuromorphic engineering' was first introduced by an American scientist Carver Mead [1]. NE has two directive goals; one is to understand the computational properties of biological neural systems using models and the other is to exploit the known properties of biological systems to design and implement efficient devices for engineering applications (C S Thakur, et al., 2018[2]). NE term is used for all neuro-inspired techniques: hardware, algorithms, and recently this discipline has emerged amongst top technologies (information is given by the world economic forum [3]). The market for neuromorphic systems is expected to increase by roughly 1.8 billion dollars by the time 2025 [4], [5]. Also due to the gigantic increase in the internet of things (IoT) and AI, the need for a system is going to increase. A review paper [6] shows a roadmap for future development in neuromorphic systems that mainly focused on the role of dendrites in neural systems. The neural emulating hardware should be highly energy-efficient (low power), parallel and efficient computation capable, and should occupy a small chip area. To achieve all the above-mentioned properties, during this decade neuromorphic engineers instead of digital computation, are looking for solutions in the analog domain. Several Si-based analog circuits for synapse modeling, learning methods, neural spike generation, etc., have been developed [7,8,9]. With the use of such compact models, digital communication (large-scale neural networks) of spiking information has also been developed which closely emulates the nature of

the human brain [10]. Single silicon transistor was interfaced successfully with neural networks, resulting in potentially interesting clinical applications for neuro-engineering systems, neuro-prosthetics, and neuro rehabilitation (F D Broccard, et al., 2017[11]). Floating-Gate-based metal oxide Semiconductor (FGMOS) devices are very well known for memory application and other low-power analog computation circuits. Recently they find applications in analog circuits that are used for neuron modeling [12, 13], competitive learning systems [14], implementation in learning algorithms [15], and implementation of online unsupervised deep learning systems [16]. Carver Mead noticed that the Si MOSFET operating below threshold in current mode has similar characteristics as "sigmoidal current-voltage", which is similar to characteristics of neural electrical(ion) channels [17]. Single MOSFET at sub-threshold consumes very less power and can become on-chip programmable, and self-adaptable using floating-gate technology. The physics of this device led to the advancement of "Neuromorphic" silicon neurons (SiNs). Neuromorphic circuits (NC) using SiNs and simulating cognitive features like learning, training, and adaptation, gained momentum in the recent decade (electric signals, V/I, and ionic signal Na/K) [18, 19]. NC emulating features like Homeostatic intrinsic plasticity, Spiking-timing-dependent plasticity (STDP), Least-mean square, perceptron, backpropagation, spiking-driven synaptic plasticity and structural plasticity [20, 21, 22, 23] have also been developed. Moreover, neural computation for artificial intelligence requires complex integrated circuitry, for which the designs need to be scaled down. Scaling of such SiNs has several advantages like higher frequency response, lower parasitic capacitances, and lower power consumption along with some design challenges [20]. Such compact efficient adaptive neural models are implemented in neuromorphic circuits which can either be used to understand the computational properties of the biological neural system or to exploit known properties (AI algorithms) of the biological system to develop intelligent machines, as illustrated in figure 1. Thus, we propose a floating gate-based PMOS (SiN) simulation model at 45nm CMOS technology which shows learning, storing, and self-adaptation with higher accuracy and stability. The model can also emulate neuron features like Spike-timing-dependent-plasticity (STDP) generation and self-adaptation (Structural plasticity). The Model shows stable learning, consumes low power, and smaller chip area. The simulated results have also been compared with previous work [20]. Our proposed SiN can be implemented in other adaptive neuromorphic circuits which in turn can be used to build a neural network emulating some partial features of the human brain. Thus, the paper is distributed as follows: section 2 demonstrates the Si Neuron model, weight concept, proposed adaptive model, and results demonstrating the learning features of neurons. Section 3 caters to indirect programming techniques of FGPMOS, and the role of equilibrium conditions in self-adaption. And in the last section, an application has been simulated. The proposed SiN model can be used to design a complete neural structure whose array can develop a neural network. Such neural networks can be used in two ways; either as an FPAA with an array of complete cell boards implanted to innovate human-like machines. Or such boards can be used to understand or emulate some part of the complex functionality of the brain. Such boards can also be used to design some assistive technology-based devices where any deficient feature of the brain can be enhanced with the help of physical implants. For example, there is a patent [24]. The invention presented here provides a well-defined and simplified method of modeling human-like thought, emotion, behavioral, cognitive, and conjectural processes.

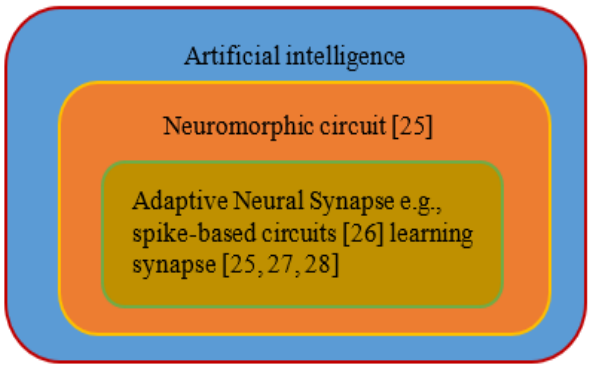

Figure 1. Neuromorphic system/ Adaptive Neuromorphic-circuits and their future in artificial intelligence.

2. The SI-based Neuron-Models

Silicon neurons (SiNs) are analog VLSI circuits that can emulate the electrophysiological behavior of neurons or in other words neuron behavior with the flow of ions. SiNs are suitable for real-time-large-scale neural emulations while in the digital domain SiNs provide only a qualitative approximation of real-time performance.

The digital domain models are not suitable for quantitative investigations. In this decade several analog domain SiN models have been developed for example Fitzhugh-Nagumo (FHN) [25], and the modified Izhikevich neuron model [26]. Memristor-based neuron models have also been proposed [27], The commercial application of neuromorphic chips includes low-power sensors, self-learning robots, and power-efficient supercomputers. Hence with scaling down of technology for power-efficient, highly integrated SiN models are designed using analog/mixed-signal circuits. Thus, some desirable properties of SiN neurons are:

- Non-volatile weight
- Compact Size
- Low power

A. B.

Proposed SiN Simulation model at 45nm technology.

Before proposing a SiN neuron model, let us consider a neuron with input x and output y in a neural network as expressed in equation 1.

$$y_n = W_{n*m} x_m \quad (1)$$

Where y_n is the output vector of size n, x_m is the input vector of size m and W is the synaptic function of size $n * m$. where weight W can be expressed as:

$$W = e^{\frac{\Delta v f g}{U_t}} \quad (2)$$

where Δv_{fg} is the change in voltage of floating gate, U_t is the thermal voltage. Our proposed SiN model generates this weight W in terms of non-volatile charge at FG which

can be programmed using few external voltages. This charge at FG can also be feedback through a capacitor, to adapt to certain changes in input stimuli. Programming this charge energy can be performed using tunneling (E_{tun}) and injection (E_{inj}) and can be expressed in terms of Δv_{fg}.

$$E_{tun} = C_{tot}\Delta v_{fg}(V_{tun} - vfg) \quad (3)$$

$$E_{inj} = C_{tot}\Delta v_{fg}(V_{ds,inj}) \quad (4)$$

Where C_{tot} denotes total parasitic capacitance, V_{tun} denotes tunneling voltage, and $V_{ds,inj}$is high drain-source voltage applied for injection.

The circuit illustrated in figure 2 is inspired from [28] which uses the two-quantum mechanisms; Fowler Nordhiem tunneling and Hot-electron Injection (IHEI) which are responsible for adding and removing electrons on the floating gate, respectively. The programming of stored charge at FG is used to adapt its dc operating point with the help of external voltages. In the simulation model of directly programmable FGPMOS, a PMOS with common FG is used as a MOS capacitor, to provide tunneling junction M_a (shown in Fig 2), which is used to form a high potential terminal for tunneling of charge from FG.

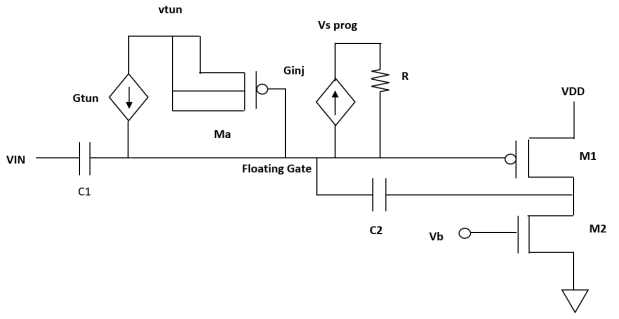

Figure 2. Low power compact, adaptive, non-volatile weight SiN simulation model.

The two-quantum current in the femtoampere range has been simulated using empirical equations (10, 11), implemented with the help of two voltages controlled current sources. Capacitor C_1, the input capacitor simulates the feature of the double polysilicon structure used to fabricate FG and control gate. Capacitor C_2 is used to provide feedback at the drain terminal. On applying external voltages at tunneling junction V_{tun} Through a MOS capacitor and a potential difference between source and drain terminal of FGPMOS, both injection and tunneling currents have been generated. The steady-state is reached when the injection current is nullified by tunneling current i.e., $I_{tun} = I_{inj}$ and thus after equilibrium (12ps) charge at the FG gets fixed.

The circuit is inputted by an up-going and down-going step at the gate terminal, Figure 3 illustrates output voltage showing adaption. The adaptation in response to the up-going pulse results in electron tunneling, which decreases charge at FG, and as a result the V_{ds} decrease which leads to less injection current. Moreover, adaptation response for down-ward going pulse results in hot electron injection that leads to increase in charge at FG which leads to increase in V_{ds} and thereby increasing the injection.

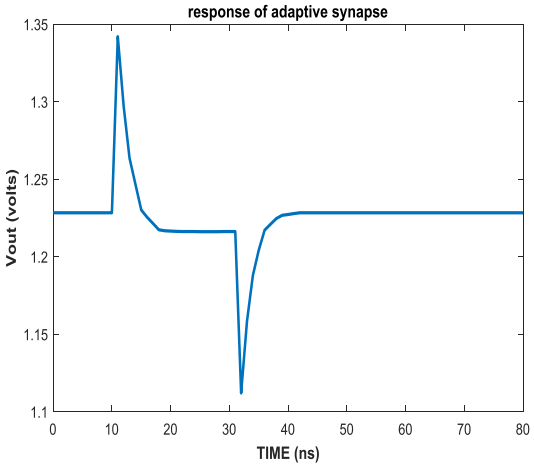

Figure 3. Illustrating adaptive output response at the drain terminal of FGPMOS.

Emulating STDP it is a biological phenomenon that provides strength to neuron wiring by adjusting the connections between the brain and neurons. The feature is based on the relative timing of a presynaptic or postsynaptic neuron's output and input action potentials in the form of spikes [29-31]. Mathematically STDP is modeled as:

$$\Delta W = \begin{cases} \Delta w^+ = A^+ e^{\frac{\Delta t}{\tau^+}}, if \Delta t > 0 \\ \Delta w^+ = A^- e^{\frac{\Delta t}{\tau^-}}, if \Delta t \leq 0 \end{cases} \quad (5)$$

Where $\Delta t = t_{post} - t_{pre}$. The equation above reflects that synapse is potentiated/raised (depotentiated) if postsynaptic action occurs after (before) presynaptic action. A^+ and A^- denote the highest change in weight and τ^+ and τ^- denote the time of interval in which spiking occurs. Weight represented in equation 5 has been simulated shown in figure 4. Which is obtained using equation 5 the plot shows weight change as a function of the time difference of presynaptic and postsynaptic spike in STDP.

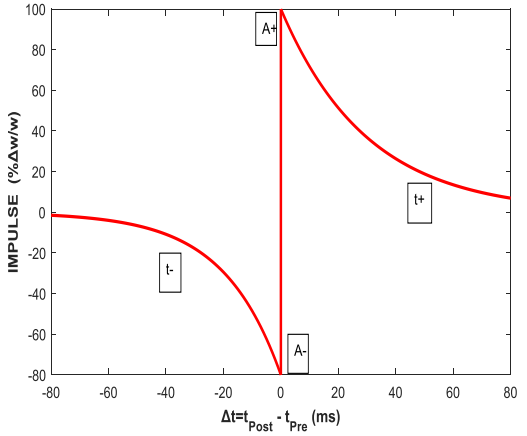

Figure 4. Plot of neuron weight extracted from equation 5.

In the previous section this neuron weight has been expressed in terms of charge at the floating gate illustrated by equation 2. whenever there is a change at the input/ programming voltages, there will be the change in charge at the floating gate terminal. The output of the neuron changes according to this change in weight multiplied by the input, which in turn results in an impulse response. It has been observed (as shown in fig 3) that the charge in FG will be adapted automatically to equilibrium position. Figure 5 represents the output voltage of the neuron model (shown in fig 2) in response to the input step. The response is similar to STDP obtained from a mathematical equation (shown in fig 4). The response is also comparable with the result of the paper [29].

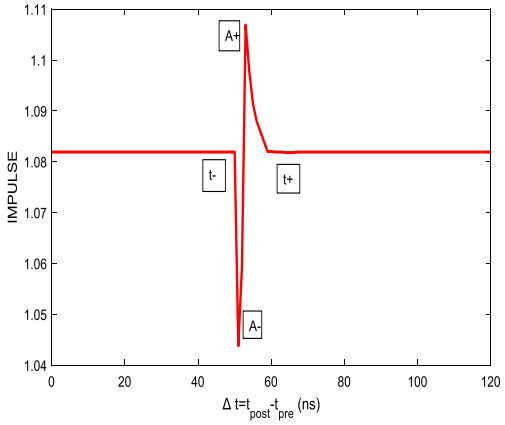

Figure 5. Emulating STDP response of neuron membrane

Extracting LMS it is the former/aged learning rule obtained for the non-spiking neural networks [23]. LMS aims to minimize error step by step with minimum change in the parameters to make the memory more efficient. For an explanation of LMS a simple neural network and adaptive linear combiner (ADALINE) have been considered and narrated by the equations as follows:

$$h = Y^{-T} W^{-} \quad (6)$$

$$e = d_s - h \quad (7)$$

Where Y^{-} represents the input vector of the neural network, W^{-} is the vector of weight, d_s are the required output and e denotes the corresponding error. LMS works on weight updating algorithm as given as:

$$\Delta W^{-} = \delta \frac{eY^{-}}{|Y^{-}|\text{^}2} \quad (8)$$

Where δ is the value chosen between 0.1 to 1 for better stability and good convergence speed and it is observed that the error reduces at every step. The main application of the LMS algorithm is to reduce mean square error at every step. This feature is used to reduce error, and to emulate neural computations and can also be designed in NCs.With the change in high potential at the tunneling junction, the amplification (dc level/equilibrium level) has been shifted, as demonstrated in Figure 6. As v_{tun} increases charge at FG decreases so the dc level for 2.11V is 1.2V and for 2.19V it is shifted to 0.95V. (The range of tunneling from 2-4V has been reduced to 2.11-2.19V). With the feedback mechanism in our proposed model if there is a difference in the desired output it is feedback to the FG terminal and hence error will be reduced step by step until the desired response is obtained.

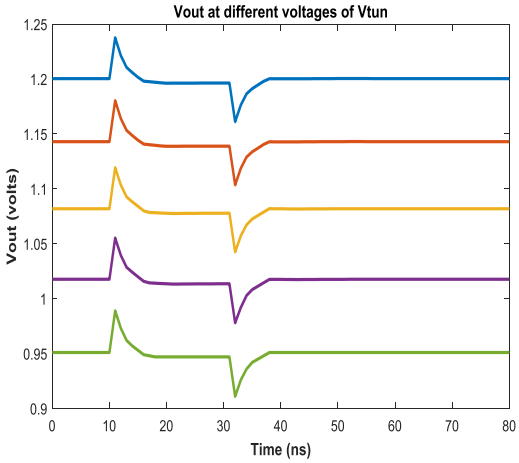

Figure 6. Shows variation of dc level on sweeping V_{tun} from 2.11v to 2.19v.

Emulating Structural plasticity: It is the cognitive behavior of the human brain. Most learning algorithms in neuromorphic systems have a definite relation to changes in synaptic weights. In the same, way the network structure (in form of wiring) of an adult brain also undergoes certain changes for example formation of new connections and replacing them with old ones and this phenomenon is known as structural plasticity (SP) [30,31]. The presence and absence of connections are treated as 1-bit memory signals and they are easy to store in CMOS latches with less power and lesser chip size [32]. These algorithms are recently applied to real-world problems. Based on SP several algorithms have been developed which have recently been applied for real- time applications [33]. The proposed model shows self-adaption of charge at the floating gate (non-volatile weight) due to feedback at the drain terminal of FGPMOS, (as shown in fig 3). This property of self-adaption of any input stimuli can depict features of structural plasticity of neurons in the human brain. In the following section, indirect programming of the proposed model has been illustrated with which model can be implemented in any neuromorphic circuit.

3. On-Chip Programming of FGPMOS

To design an array of proposed SiN neural cells as described in the previous section, to generate an output with respect to input stimuli, weights need to be estimated. As illustrated earlier these weights correspond to the charge stored in the floating gate (equation 2). The proposed SiN model is based on floating gate technology where the charge at the floating gate(weights) is programmed using external voltages using two quantum mechanical techniques; tunneling and injection. The experimental results of on-chip, precise, non-volatile programming have been demonstrated in the next section. The charge also self-adapts in correspondence to spiking input due to feedback shown in Fig 2. The FGPMOS can be programmed either directly or indirectly using

programmer FGPMOS with a common floating gate. To explain programming techniques a simulation model for indirectly programmable FGPMOS is demonstrated in Figure 7(a). In the mask shown in Figure 7 (b) floating gate has been fabricated using a double poly structure. The floating gate whose charge works like weights in our proposed SiN model is once programmed, remains trapped on it for years, as FG is covered from oxide from all sides and electronically 'floating'. The FGPMOS has been fabricated using on semiconductor C5 CMOS process using MOSIS fabrication services in the USA in association with the University of Maryland. The experimental results of tunneling and injection respectively are demonstrated in Figures 8(a) and (b), respectively. The charge at the floating gate can be programmed with seven bits of resolution as illustrated in Tables I and II. The tunneling, removal of charge, and an injection that is the introduction of charge have been simulated with the help of voltage-controlled current sources in the simulation model shown in Figure 7(a). These VCCS use empirical current equations derived f4rom experimental values and relations with the voltage differences, written in equations 10 and 11. An equilibrium is created when simultaneously tunneling and injection of charge are performed after 0.2µs, as shown in Figure 10. The final stable learned charge at the floating gate is the difference between two currents, as shown in equation 9. This change in charge after equilibrium is the stable weight of our SiN neural model and according to it will produce output when an input spike is provided. In the next section, programming techniques have been explained in detail.

$$C\frac{dvfg}{dt} = I_{tun} - I_{inj} \qquad (9)$$

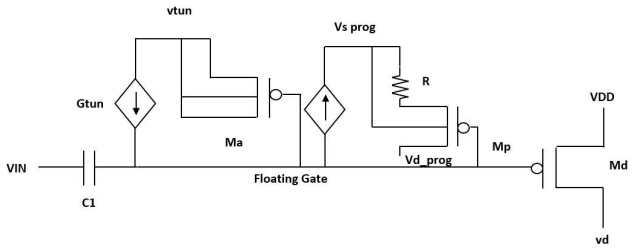

Figure 7(a). Simulation model of indirectly programmable FGPMOS (Md the FGPMOS, Mp programmer FGPMOS used for injection, MOS capacitor for Tunneling, Ma common FG separated from CG through C1 (double ploy structure), and two voltage-dependent current sources which depend on current equations (injection Iinj & Tunneling Itun derived from experimental data.

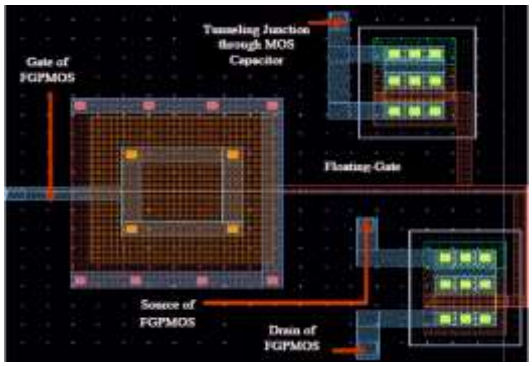

Figure 7(b). Layout of directly programmable FGPMOS.

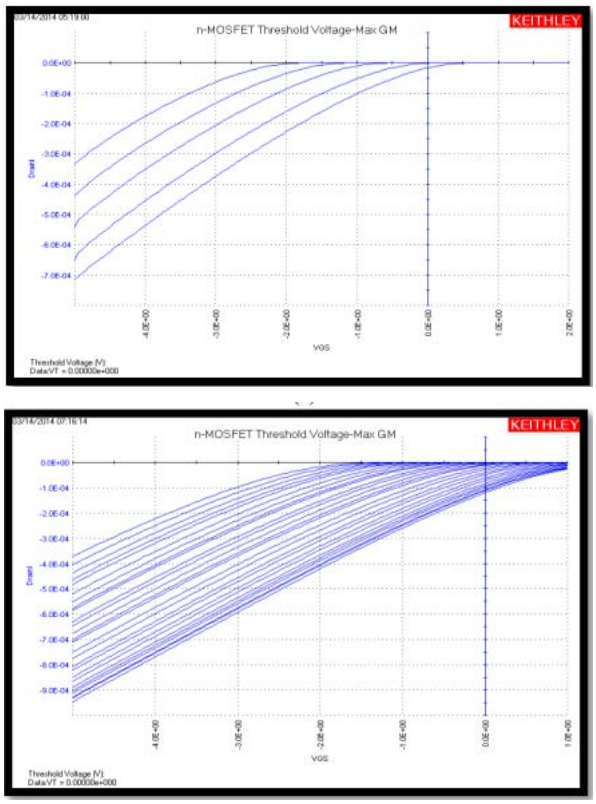

Figure 8(a). Experimental plot for programming of threshold voltage by tunneling. (b): Experimental plot for programming of threshold voltage by injection.

A. *Programming technique*

Tunneling arises from the phenomenon of the electron wave function which has a finite extent. It is a quantum mechanics process that is used to tunnel out electrons from the floating gate. For a thin barrier it is sufficient for an electron to penetrate the barrier. In Fowler Nordheim tunneling mechanism a high potential is applied at the tunneling junction to create a strong electric field between the tunneling junction and Floating gate which in turn results in a thinner barrier to the electron at the floating gate as illustrated in figure 7(a). The empirical equation (10) parameters have been extracted from hardware results and estimated for 45nm MOS model values (inspired by paper [20]).

$$I_{tun} = -I_{tun0}\, exp\, exp\left(\frac{-V_f}{V_{tun}-V_{fg}}\right) \qquad (10)$$

Where v_f and I_{tun0} are the extracted parameter and values estimated are $I_{tun0} = 2.e7, V_f = 269$. With the increase in tunneling junction voltage, the negative charge at the floating gate reduces due to which the positive threshold voltage of FGPMOS increases. The same has been illustrated in Figure 9(a), which depicts the change in the value of drain current at one time (200ps) with increasing tunneling voltage from 2V to 4V.

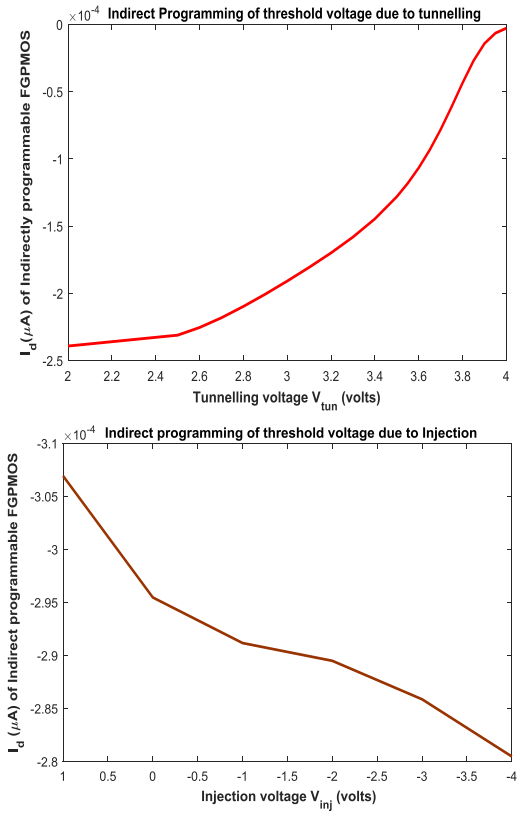

Figure 9(a). Showing variation of drain current by sweeping Tunneling voltage V_{tun} from 2v to 4v. (b) Showing variation of drain current by sweeping injection voltage V_{inj} (v_d-v_s) from 1v to -4v.

Injection Hot electron injection provides us a facility to inject electrons i.e. increases the positive charge at the floating gate. The Physics of hot electron injection is to provide electrons with enough kinetic energy and direction in the channel to drain near the depletion region to surpass the Si-SiO_2 barrier. FGPMOS must have two requirements for injection of an electron in FG. First, an electron must gain more than 3.1ev of kinetic energy to cross the Si-SiO_2 barrier. Second, the electric field in the oxide is desired in a unique direction to receive electrons once they cross the Si-SiO_2barrier. The injection current can be simulated using empirical equation 11, whose parameter values have been extracted from fabricated results [20].

$$I_{inj} = I_s \times \alpha \times exp\ exp\left(\frac{-\beta}{V_{fg}-V_s+\gamma} + V_s - V_d\right) \quad (11)$$

Where $\alpha = 0.5e-8, \beta = 150, \gamma = 0.402$ have been estimated for the proposed model at 45nm. For indirect injection, a programmer uses a PMOS at common floating gate. With the increase in the magnitude of the difference of voltages between drain and source, the negative charge at the floating gate increases and the threshold voltage of FGPMOS decreases. The same has been illustrated in Figure 9(b), which depicts the change in the value of drain current at one time (1000ns) with increasing V_{inj} voltage from 1v to -4v.

Table. I Tunneling programming precision

V_{tun}(Volts)	V_{fg}(Volts)
3.0000001	1.2851
3.0000002	1.2852
3.0000003	1.2853
3.0000004	1.2854
3.0000005	1.2855
3.0000006	1.2856
3.0000007	1.2857

Table. II Injection programming precision

V_{inj}(Volts)	V_{fg}(Volts)
3.0000001	1.3856
3.0000002	1.3857
3.0000003	1.3858
3.0000004	1.3859
3.0000005	1.3860
3.0000006	1.3861
3.0000007	1.3862

Injection and tunneling current is tuned with voltage-controlled current sources (VCCS) the value of VCCS depends upon tunneling and injection voltages according to the empirical current (equations 10 and 11), Due to the tunneling/Injection, quantum mechanism V_{th} of the FGPMOS can be programmed with about 7 bits of programming resolution. In papers [34, 35] it has been said by experimental verified results that with tunneling/injection mechanism Vth of FGPMOS is programmed by about 13 bits of programming resolution. Same has been observed while simulation and is illustrated in Table I and Table II which depict the change in drain current on increasing V_{tun} from 3.0000001v to 3.0000007v and this change is due to a change in voltage of the FG respectively.

Equilibrium Condition injection and tunneling mechanism are operated at the same time and it is being noticed that the effect of injection on the charge at the FG (the value of V_{th}) is more as compared to the tunneling. Equilibrium operating conditions has been fulfilled where both process effects get neutralized. To attain equilibrium between injection current and tunneling current floating gate voltage is varied from 0.8v to 2 v and as illustrated in figure 10.

Equilibrium is attained at V_{fg}=1.05v which concludes that the equilibrium condition is attained at two values of V_{fg}.

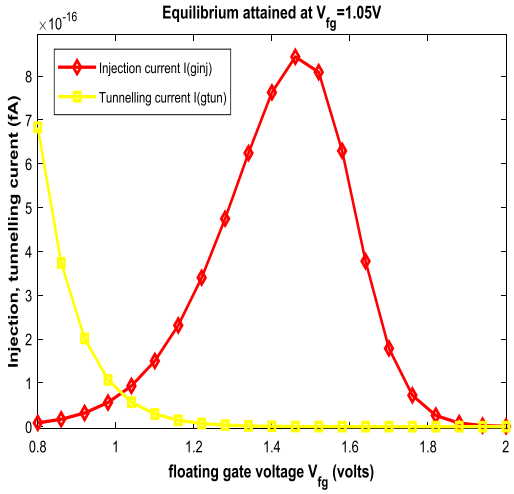

Figure 10. Plot of injection current (I_{inj}) and tunneling current (I_{tun}) w.r.t floating gate voltage (v_{fg}).

4. Biosensor Circuit with Proposed SIN

Neuromorphic circuits simulating spikes (STDP) have recently become a popular area of interest in the neuro-engineering field (Stephen Nease et al., 2016). These designs are also used to implement event-driven computing systems. Within the above context many different types of SiNs have been proposed that mimic neurons and synapses at different levels [36]. A Neuromorphic biosensor circuit is used to detect the functioning of biomolecules; sodium and potassium. It generates an output whose frequency is modulated with different current values. It consists of an FG-FET sensing area, a membrane capacitor C_M, a N_A sodium channel, and a potassium K channel. Whenever any charge particle appears around the sensing area of the circuitry the threshold voltage of FG-FET gets changed and due to this there is a drain current variation across the drain terminal of FG-FET, which results in a spike at the membrane capacitor with the help of feedback Na and K sub circuits [37]. The FG-FET with bio-sensing area in the circuit is replaced with our proposed self-adaptive FGPMOS model as shown in Fig 11. The circuit consists of two feedback sub-circuits: sodium feedback circuit and a potassium feedback circuit. The sodium (Na) channel shown in figure 11 works like a bandpass filter; the bias voltage V_M and V_H is used to tune the bandpass filter circuit. The current across the sodium (Na) channel in response to a step input is shown in figure 12(a). Further, the potassium (K) channel whose gate voltage is controlled by MOS M6, M7 and C3 as shown in figure 11. The K feedback circuit works like a low pass filter, and the tuning of the time constant of the potassium (K) channel is done with the help of biasing voltage Vn. Moreover, the current across the potassium (K) channel is shown in figure 12(b). With the adaptive SiN model, any input pulse can generate self-adaptive impulses at the membrane capacitor which can further be controlled by feedback from Na and K circuits. The charging of the neuron membrane can be done by the Na channel, while the discharging of the cell membrane (CM) happens through the K channel. Thus, the complete biosensor design is used not only to emulate STDP depicting effects of Na/K ions in neuron membrane but also used to emulate features of structural plasticity (self-adaption) of the human brain. The spike generated at the cell membrane as shown in figure 12 can be used to improve the insulation of the myelin sheath which is responsible to transmit electrical impulses in the brain and spinal cord and have the ability to emulate the STDP feature of the human brain.

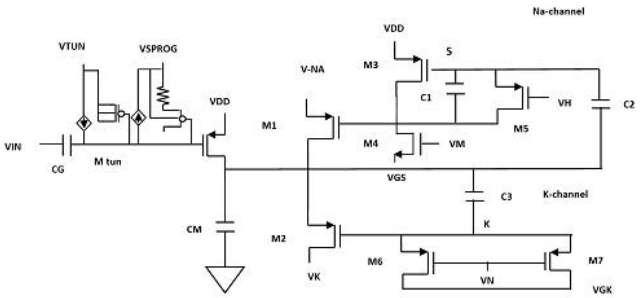

Figure 11. Bimolecular Sensor circuit using neural synapse FGMOS.

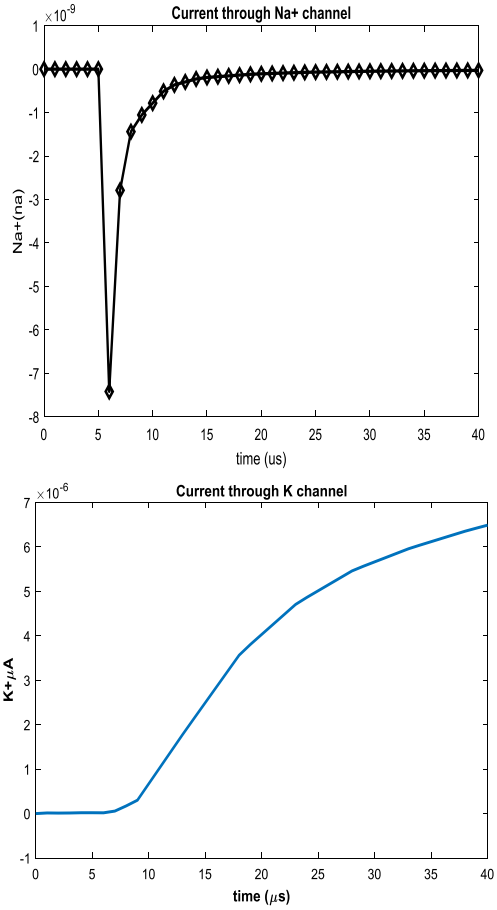

Figure 12 (a). Current across sodium channel (b): Current across potassium channel.

4.1 Action Potential

The action potential is an electrical activity that occurs when different types of ions cross the membrane of our neuron. In response to the stimulus provided at the input the sodium channels open as there are more sodium ions outside the neuron membrane and generally neuron has negative relative to outside of the neuron membrane, depolarization occurs because sodium ion is positively charged and due to this neuron becomes more positive and as a result of this potassium channel takes more time in opening and when they do so potassium ions rushes out of the neuron membrane, reversing the process of depolarization also at this particular instant sodium channels starts to close. When the neuron is not sending any signal in the form of spikes it is considered to be at rest, the resting potential of a neuron is (-70mV) which represents that the outside of the neuron membrane is 70mV higher than the inside. This causes the action potential to reach -70mV (re-polarization) but actually, it goes beyond -70mV because the potassium channel opens a bit too long and this state is stated as hyperpolarization and then the cell returns back to resting potential at -70mV.

Action potential shown in figure 13 is obtained by applying a step pulse from (-65mV to -10mV) at the input terminal of the bio-sensor circuit shown in figure 11. It can be noted that due to tunability of circuit and bias conditions a significant variation in the shape of the action potential is observed. The voltage shown across the y axis of figure 13 is the voltage spike at the cell membrane (C_M) minus the voltage of the circuit at rest. The concept of depolarization (rising phase) where the spike goes to +40µV and Repolarization (falling phase) is illustrated in figure 13.

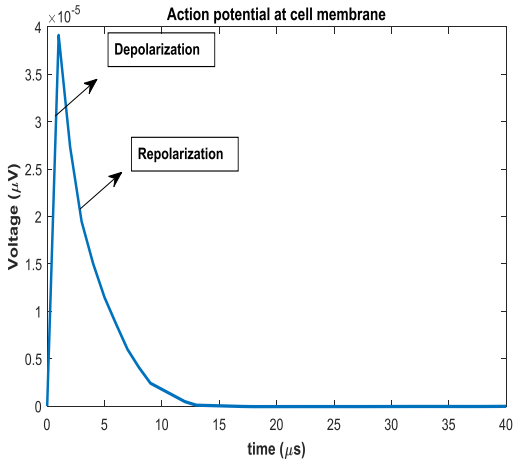

Figure 13. the plot represents voltage across membrane capacitor (C_M) shown in fig 11. Output response across cell membrane.

5. Conclusion

In this paper a Si-based adaptive neuron model is proposed and simulated using 45nm CMOS technology. It shows features like storing, programming, and adaptability of charge at FG. It can enhance the on-chip learning ability of Si neurons. The model shows 4.5uV/℃of temperature coefficient when the temperature is varied from 0 to 80-degree Celsius, consumes 0.675µW power, and occupies a chip area of about 130×90 nm^2. Thus, a single FGPMOS operated at subthreshold conduction, is used to emulate a neuron and its features such as LMS, STDP, and structural plasticity. The proposed synapse model along with the concept of proposed cell membrane could illustrate short-term synaptic action of a cell in response to input spike. The work can be extended by adding an axon and dendrite circuit with the proposed cell model and a complete neural architecture can be created. An array of these cells depicting features like learning, storing, and self-adaption can create a Neural network. Such analog based Neural networks can be used in two ways; 1. it can get implanted in machines to depict human-like behavior in bots. 2. It can also be implanted inside a deficient brain to replicate the correct cognitive behavior (can help in developing devices for assistive technology).

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