Design and FPGA Implementation of Efficient Multiplier Architecture using Reversible Logic

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Abstract: - In the present scenario in wireless communication, portable and mobile devices have consistently demanded the designer to design the device for low power consumption and fastest data path computations at low cost. Power loss and time delay become a major parameter in integrated circuits, which plays a very crucial role in digital signal processing operations in communication systems. One significant issue in the existing system is its binary nature, relying on true or false values without accounting for the nuances and uncertainties present in many real-world situations. In comparison to the current method, the reversible logic-based multiplier is suggested to increase multiplication's speed, area, and power. Reversible logic offers a one-to-one mapping between input and output states, ensuring the preservation of information. Reversible logic circuits are intrinsically more energy-efficient because of this property. The proposed architecture will be synthesized and simulated using Xilinx with various FPGA boards. Finally, compare the results with the existing technique. The synthesis result shows that the speed of proposed multiplier based on reversible logic gets improved as compared to Array multiplier (35.83%), Wallace tree multiplier (34.58 %), Vedic Multiplier based on CLA (28.49%), Vedic Multiplier based on RCA (20.65%), Booth Multiplication (21.65%) and Vedic Multiplication based on HCA (20.10%) and Hybrid multiplier using CSELA (17.81%) and Hybrid Vedic Multiplier (7.15%).

Key-Words: - Reversible logic, information loss, low power consumption, FPGA, Multiplier ,Speed, Area, Power.

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1 Introduction

The rapid advancement of technology is significantly influencing engineering innovation. The construction of a unique and sophisticated electronic product is made possible by the technological transition, which also opens up new avenues for the use of engineering. More than ever, multipurpose headsets, cameras, and handheld computers must have excellent accuracy and performance. Apart from the standard enhancements in performance, users are also taken into consideration regarding battery life, reliability, and environmentally friendly computing. As these goods advance, having several features, great performance with little energy use, portability, and low cost are crucial objectives. Reducing the size of the key circuit components is a modern prototype to achieve these goals. The transition from high-level technology generation to low-level

Multipliers and Adders are the key components of digital filters which are the main contributors to chip area, power, and delay for each operation. Generally, the adders/Multipliers in digital filters have a large delay, large area utilization, and consume huge amount of power consumption. Hence the main objective is to design a multiplier/adder with less delay and less power consumption, [1], [2], [3].

Several literature on optimizing the critical path delay, and reducing the utilization of power or size of the ALUs have been investigated. The constraint of less delay with lowest power utilization is the crucial factor which is the biggest task for any designer. Not possible to design an ALU without adders as they are key component modules. Hence the operating time and power/energy utilization of an adder strongly impact the speed and power utilization of the processor architectures. Therefore,

optimization of the adder's performance, optimized the performance of the whole system significantly, [4].

In modular arithmetic, this is used in cryptography/ test vector generation algorithms. In that modular exponentiation/ multiplication/ additions are frequently used for arithmetic operations. In these applications, three operand adders are a basic building block, [5]. The idea looks at the technologies required to support a smart ambulance system and considers the advantages and disadvantages of putting it into practice. It also looks at how the idea might be used in the future, including remote monitoring and diagnostics. Such a technological introduction would have far-reaching effects and could transform the way that ambulance services are currently provided. Conclusively, the Smart Ambulance initiative, powered by LoRa technology, signifies a noteworthy advancement in the pursuit of enhanced emergency medical services, [6], [7]. This creative project has a clear goal of saving lives and cutting down on hospital travel time, and it has the potential to completely change how we handle serious medical situations. The foundation of our work is LoRa technology, which makes smooth, real-time communication possible. This is critical for providing care quickly and effectively. The ones that follow will explain the nuances of the Smart Ambulance project's implementation as we set out on this journey into its core and demonstrate how technology and human compassion can work together for the greater good. Our shared goal is to improve the lives of those in extreme need by not only reducing response times but also inspiring hope in the face of hardship.

2 Literature Survey

This chapter provides detailed study of present technologies in the current research area.

Proposed a New High Speed Multiplier based on Carry Look Ahead Adder and Compressor. The proposed method was to increase the speed of arithmetic computation using a compressor and carry-look-ahead (CLA) adder. In that method, the number of full adders was reduced by introducing compressors. The CLA was used to reduce the carry generation time in a single instant. The performance (speed in terms of delay) of the proposed multiplier was enhanced as compared to the exact multipliers. The 32-bit approximate multiplier was designed/ simulated using the proposed technique and obtained a 20.67us delay; it has 5% less than the exact multiplier, [8], [9].

Proposed a carry look ahead adder based on two efficient reconfigurable architectures of the adder, [10]. The Adder-I was developed using Four bit CLA module with a new approximate sum generation. Whereas, the adder II was designed using a new complementary logic-based CLA module, which develops developed the proposed new logic formulation. The proposed design of adders can achieve high performance with low cost and acceptable loss in quality. The proposed method was simulated on TSMC 65nm technology, which improved the hardware utilization to 76% and 80% for adder 1 and adder 2 respectively, and similar speed as 71% and 74% for adder 1 and adder 2 respectively over the best existing CLA based approximate adder, [11], [12].

The efficient approximate Carry Select Adder was proposed. This adder was used to eliminate the carry 1 input path in LSB and achieved an increased speed and reduced hardware utilization. Also, this approximate adder utilized an algorithmic module split-up technique which increased the speed in all places of the circuit. The approximate carry select adder design consists of approximate full adder blocks with a reduced number of gates and utilization of power. The approximate carry select adder had reduced area utilization, increased the speed of operation, reduced error percentage, and power delay product than exact and present adders.

A new High Speed and Area Efficient Wallace Tree Multiplier based on Square Root Carry Select Adder with Mirror Adder was proposed. In this technique, the SQRT CSLA block was redesigned by replacing Ripple Carry Adder blocks to mirror adder and Binary to Excess One Converter (BEC) in order to attain high performance and less area utilization. This multiplier was designed using Verilog HDL and implemented /verified using the Xilinx ISIM simulator. Also this multiplier is compared with the existing multiplier in terms of the number of LUTs and delay (ns), [13]

Different topologies of multiplier and adder for FFA-based FIR structures was implemented. In order to optimize computation, the architecture of various multipliers such as the add and shift technique, Vedic, and booth multiplier techniques were developed. Different architectures of adder like carry select adder, carry save adder, and Han-Carlson adder are examined to enhance the performance of the FFA structure. The performance tradeoffs between the area, delay, and power

dissipation of this multiplier were investigated, [14].

An energy-efficient approximate adder based on a novel hybrid error reduction technique was proposed, [15]. It considerably improved the accuracy of arithmetic operation and also very low cost without extra overheads of power and area utilization. This proposed hybrid error minimization technique utilized only 2 input bits and adjusted the approximate outputs to minimize the error distance, so that the overall accuracy was improved. The proposed technique was implemented using 65-nm technology; it had better three, two, and two times in energy, power, and area efficiencies, respectively than accurate adders. Particularly, the proposed adder minimized the power, energy, and error delay- product utilization of 51%, 49%, and 47% respectively.

An Energy efficient technique for the multiplication of 2's- complement binary numbers with the two least significant bits was proposed. The double LSB arithmetic has many advantages, they are symmetric representation range, negation carried out only by bitwise inversion, and the reduced the complexity of rounding process in the floating point architectures. The proposed technique was implemented at 45 nm, in that 3.1 % and 3.3% energy overhead are improved as compared to the conventional Modified Booth multiplier. Also, 10.2% energy and 7.8% area gained as compared to the previous state-of-the-art implementation, [16], [17].

The performances are majorly factored by their speed of arithmetic computation. In any arithmetic computation Adders, Shifters, and Multipliers are the essential building blocks of any Digital Signal Processor (DSP) architecture. In addition, process due to large carry propagation delay and sequential behavior, conventional digital system architecture is sluggish in nature. Also, Multiplication dominates the execution time of most DSP applications hence there is a need for a high speed multiplier for designing efficient data path circuits. The most effective way to increase the speed of a multiplier is to reduce the number of partial products because multiplication precedes a series of additions for the partial products.

Furthermore, the decrease in chip size and increase in chip density in that complexity escalate the difficulty in designing higher performance and low power consuming systems on a chip. Further, overall power management on a chip is becoming a big challenge below 100 nW because of its increased design complexity.

In submicron technologies, leakage, and dynamic power consumption is becoming an essential design parameter as it is dissipating a considerable portion of the total power consumption. Reducing power is a preternatural development that gathered importance with the developments of deep submicron nodes and nanometer technologies. Hence design of arithmetic building blocks to dissipate less power is of utmost importance in digital system design. In order to reduce this power dissipation, there are many low-power approaches such as multiple threshold voltage, reducing the voltage swing, clock gating, use of reversible logic gates, etc.

3 Existing System

In digital systems for processing images, signals, and videos, adders have a major role to play. Because they are impacted by the system's performance and require additional mathematical operations, such as division and multiplication. Therefore, the primary crucial characteristic in terms of delay for these signal processing procedures is speed. One of the main needs in signal processing applications is a high-speed adder, [18], [19], [20].

An adder's main purpose is to accept two binary values as input and output a binary sum. Usually, the numbers are shown as binary, which is made up of 0s and 1s. Based on their unique construction and capabilities, adders can be categorized into a number of different varieties, such as ripple-carry adders, half adders, and complete adders, [21].

3.1 Carry Look Ahead Adder (CLA)

A greater number of stages in RCA will result in increased latency. In order to reduce this delay, the Carry Look-Ahead Adder (CLA), another adder, was invented. By introducing the create and propagate terms to identify each output carry bit separately, this adder is operating at a faster pace. The Figure 1 depicts the CLA structure.

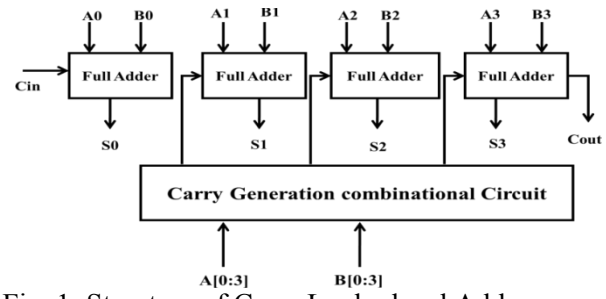

Fig. 1: Structure of Carry Look-ahead Adder

Depending on the restrictions that each application has, the multipliers can be utilized for a variety of purposes. Examining the area, power, and speed parameters of the multiplication employed in the signal processing module is therefore essential, [22].

When multiplying two binary values, there are many different kinds of multipliers to take into account.

Another binary multiplication technique is the Wallace multiplier. It multiplies the two integers in terms of binary. This Wallace tree multiplier is fast compared to the binary array multiplier. It is one of the parallel multipliers, which uses the carry save addition algorithm to reduce the delay. This technique reduces the partial product stage to two rows with the help of half adders and full adders, [23]. Finally, the carry save adder is used to add the partial product of two rows.

Wallace tree multiplier, the following steps to perform the multiplication of two numbers.

- Partial product generation.
- Reducing the partial products to two rows with the help of half adders and full adders.
- Finally, add these two rows using a fast adder.

The above steps are diagrammatically represented and shown in the Figure 3.

Due to its nonlinear height of the partial product stage, the Wallace tree multiplier outperforms the array multiplier in terms of speed. However, the structure becomes more convoluted and erratic as the number of adders increases.

As a result of the structure's complexity, the designer is steering clear of it. This approach employs a speedier, but erratic, partial product tree reduction. For low-power applications, these topologies are typically avoided because more wiring equals more power usage. For massive bit multiplication, nonetheless, it performs quicker than the Carry save adder. This multiplier's drawback is that it is highly erratic, which makes the layout structure more difficult, [23]. In comparison to an array multiplier, there is a greater number of hardware requirements, but the multiplier's delay is decreased.

4 Proposed System

A particular method of designing digital logic circuits called reversible logic aims to build circuits that allow information to be processed and "undone" without any information being lost. Operations like AND, OR, and NOT in conventional digital logic are irreversible, which means that it is difficult to readily reverse them in order to recover the original input values.The block diagram of reversible Logic is shown in Figure 2. Reversible logic aims to preserve information, making it valuable in low-power computing, quantum computing, and other fields where information preservation and energy efficiency are crucial.

An unsigned array multiplier is a digital circuit designed to multiply two unsigned binary numbers, producing the product as its output. This type of multiplier is extensively used in digital arithmetic and serves as a fundamental component in many computer systems and applications, including microprocessors, digital signal processors, and various mathematical computations. It performs binary multiplication by taking two binary numbers and generating their product.

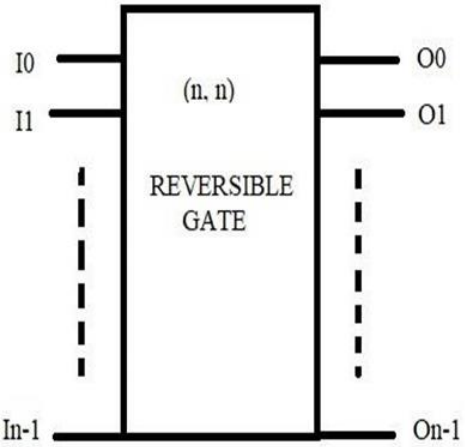

Fig. 2: Reversible Logic

Unsigned numbers are always considered positive, and their most significant bit (MSB) does not represent the sign. This contrasts with signed numbers, where the MSB is used to indicate whether the value is positive or negative.

Array multiplication utilizes an array of AND gates to compute partial products, which are then accumulated using an array of adders to determine the final result. This method enables the multiplication of unsigned binary numbers by breaking the process into a series of bitwise operations. Each bit of one number is multiplied by each bit of the other number, and the resulting partial products are added together, considering carry bits. One of the key advantages of the unsigned array multiplier is its simplicity and regular structure, which makes it suitable for hardware implementation. However, it can be slower and require more hardware resources compared to other multiplication algorithms,

especially for very large ones.The block diagram of proposed multiplier using Reversible logic is shown in Figure 3 (Appendix).

In summary, an unsigned array multiplier is a fundamental digital circuit used for multiplying unsigned binary numbers. While it has its advantages in terms of simplicity and regularity, it may not be the most efficient option for high-performance applications. Nonetheless, it remains a crucial building block in digital arithmetic units and serves as the basis for understanding more advanced multiplication algorithms and hardware structures.

5 Results and Discussions

All the existing multipliers are surveyed and proposed multiplier designs are. These multipliers are simulated / synthesized in XILINX ISE using Verilog HDL and implemented the same in FPGA devices. All the multipliers are simulated, synthesized, and verified separately. The simulation result and Device utilization summary of the Existing Multiplier are shown in the Figure 4 (Appendix).

Table 1 (Appendix) shows that the Comparison Result of different Multiplier with Spartan6 FPGA.

6 Conclusions and Future Scope

This research explores the creation of reversible adders using a variety of reversible logic-based multiplier architectures. Comparing the results to the current multiplication methodology, it was evident that the reversible logic-based multiplication method significantly improves multiplication speed while reducing size. Xilinx software is utilized to generate and simulate the suggested Reversible logic-based multiplier design, which is then successfully implemented on FPGA boards. The synthesized result shows that the delay of proposed Reversible logic-based multiplier is improved 35.83%, 34.58%, 21.65%, 28.49%, 20.65%, 20.10%, 17.81%, 07.15% as compared to Array Multiplication, Wallace tree multiplier, Booth Multiplier, Vedic Multiplier using CLA, Vedic Multiplier RCA, Vedic Multiplication using HCA, Hybrid Multiplier using CSELA and Hybrid Vedic Multiplier respectively. This work will focus on large operand size of the multiplier, image processing, and multimedia applications in the future.

This innovative approach not only contributes to sustainable and energy-efficient hardware design but also opens up exciting avenues for further exploration in reversible logic-based circuitry, promising advancements in the field of digital signal processing and digital system design.

Declaration of Generative AI and AI-assisted Technologies in the Writing Process

During the preparation of this work the authors used Grammarly for language editing. After using this service, the authors reviewed and edited the content as needed and take full responsibility for the content of the publication.

References:

[1] V.Thamizharasan and N. Kasthuri “High speed Hybrid Multiplier design using a Hybrid adder with FPGA implementation," in *IETE journal of research*, Vol. 69,no.05, pp. 2587-2594 (2023), https://doi.org/10.1080/03772063.2021.1912655.

[2] Kalaiselvi, C.M., Sabeenian, R.S. A modular technique of Booth encoding and Vedic multiplier for low-area and high-speed applications. *Scientific Reports*, Vol.13, PP.22379 (2023). https://doi.org/10.1038/s41598-023-49913-5.

[3] S Sasikala, S Gomathi, M Kanimozhi, KS Lakshana, R Karthik “Performance Analysis of a Low-Power High-Speed Hybrid Multiplier Circuit ," in *International Journal of Advanced Trends in Computer Science and Engineering* , Vol.9,no.3 pp 3793-3797 june.2020. https://doi.org/10.30534/ijatcse/2020/197932020.

[4] S. Dhanasekar, P. Malin Bruntha, L. Jubair Ahmed, G. Valarmathi, V. Govindaraj (2012). An Area Efficient FFT Processor using Modified Compressor adder based Vedic Multiplier. *6th International Conference on Devices, Circuits and Systems*, Coimbatore, India,62-66. (2022). https://doi.org/10.1109/ICDCS54290.2022.9780676.

[5] M Parimaladevi, & R Karthi “Analysis of Power Efficient Modulo 2n+ 1 Adder Architectures ," in *International Journal of Computer Applications*, Vol.70,no.4, pp.8-16,2013. http://dx.doi.org/10.5120/11948-7765.

[6] Gomathi Swaminathan, G Murugesan, S Sasikala, L Murali “A novel implementation

of combined systolic and folded architectures for adaptive filters in FPGA," in *Microprocessors and Microsystems*, Vol.74, 103018, 2020. https://doi.org/10.1016/j.micpro.2020.103018

[7] Thamizharasan, V., Parthipan, V. Design of efficient binary multiplier architecture using hybrid compressor with FPGA implementation. *Scientific Reports*, Vol. 14, pp.8492 (2024). http://dx.doi.org/10.21203/rs.3.rs-3787695/v1.

[8] Priyadharshni, M., Chathalingathu, A., Kumaravel, S.. Logically Optimal Novel 4:2 Compressor Architectures for High-Performance Applications. *Arab J Sci Eng*., Vol.45, pp.6199–6209 (2020). https://doi.org/10.1007/s13369-020-04503-9.

[9] S.Danasekar "An area efficient vedic multiplier for FFT processor implementation using 4-2 compressor adder," in *International Journal of Electronics*, Vol. 111, no.6, pp 935–951,2023. https://doi.org/10.1080/00207217.2023.2278434.

[10] K. Sivanandam and P. Kumar "Design and performance analysis of reconfigurable modified Vedic multiplier with 3-1-1-2 compressor," in *Microprocessors and Microsystems*, Vol. 65, pp. 97-106,2019. https://doi.org/10.1016/j.micpro.2019.01.002.

[11] J. Kandpal, A. Tomar, M. Agarwal and K. K. Sharma, "High-Speed Hybrid-Logic Full Adder Using High-Performance 10-T XOR–XNOR Cell," in I*EEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 6, pp. 1413-1422, June 2020. https://doi.org/10.1109/TVLSI.2020.2983850

[12] Shamim, and C. Saurabh, "Modified Binary Multiplier Circuit Based on Vedic Mathematics," in *2019 6th International Conference on Signal Processing and Integrated Networks (SPIN)*, Noida, India 234-237 May, 2019. http://dx.doi.org/10.1109/SPIN.2019.8711583.

[13] Hussain, C. K. Pandey and S. Chaudhury, "Design and Analysis of High-Performance Multiplier Circuit," *2019 Devices for Integrated Circuit (DevIC)*, Kalyani, India, Mar.2019, pp. 245-247. http://dx.doi.org/10.1109/DEVIC.2019.8783322.

[14] S. N. Gadakh and A. S. Khade, "FPGA implementation of high speed vedic multiplier," *International Conference & Workshop on Electronics & Telecommunication Engineering (ICWET 2016)*, Mumbai, 2016, pp. 184-187, doi: 10.1049/cp.2016.1144.

[15] S. M. Cho, P. K. Meher, L. T. Nhat Trung, H. J. Cho and S. Y. Park, "Design of Very High-Speed Pipeline FIR Filter Through Precise Critical Path Analysis," in *IEEE Access*, vol. 9, pp. 34722-34735, 2021. https://doi.org/10.1109/ACCESS.2021.3061759.

[16] P. Lyakhov, M. Valueva, G. Valuev and N. Nagornov, "High-Performance Digital Filtering on Truncated Multiply-Accumulate Units in the Residue Number System," in *IEEE Access*, vol. 8, pp. 209181-209190, 2020. https://doi.org/10.1109/ACCESS.2020.3038496.

[17] Prasath K.S.R., & Subhendu K,S., (2017). An approach for fixed coefficient RNS-based FIR filter. *International Journal of Electronics*, 104(8), 1358-1376. https://doi.org/10.1080/00207217.2017.1296593.

[18] Krishnakumar.S And Ansiya Eshack," Reversible logic in pipelined low power vedic multiplier" *Indonesian Journal of Electrical Engineering and Computer Science*. Vol.16, no.3,pp 1265-1272. http://doi.org/10.11591/ijeecs.v16.i3.pp1265-1272.

[19] Chaluvadi Prasanth,. Mante Anil, Kolla Sahithi and K. Vijay Raviteja (2018) 'Design of Low-Power Reversible Carry Select Adder using D-Latch ,'in *International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering*, Vol. 5, no. 4, pp. 52-57 10.17148/IJIREEICE.2017.5410.

[20] Yuganghar.K , Tejkumar.M, Ganesh.V Raja And Siva .D,"High Performance Array Multiplier Using Reversible Logic Structure." 2018 International Conference on Current Trends towards Converging Technologies (ICCTCT), Coimbatore, India. https://doi.org/10.1109/ICCTCT.2018.8550872.

[21] Vuppala Chandralekha, Latchpatula Navya,neelam Syamala And Kishore Sanapala,"Design of 8 Bit And 16 Bit Reversible ALU For Low Power Applications." *2020 IEEE 5th International Conference on Computing Communication*

and Automation (ICCCA), Greater Noida, India. http://dx.doi.org/10.1109/ICCCA49541.2020.9250876.

[22] Beechu Naresh Kumar Reddy,(2020) 'Design and implementation of high performance and area efficient square architecture using Vedic Mathematics,' *Analog Integrated Circuit Siginal Process*, Vol.102, pp.501–506. https://doi.org/10.1007/s10470-019-01496-w.

[23] Boppana,K. Kommareddy, J. and Ren,S.(2019) 'Low-Cost and High-Performance 8 × 8 Booth Multiplier,' *Circuits System Signal Process*, Vol. 38, no.9 pp.4357– 4368. https://doi.org/10.1007/s00034-019-01044-x.

Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The authors equally contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

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Conflict of Interest

The authors have no conflicts of interest to declare.

APPENDIX

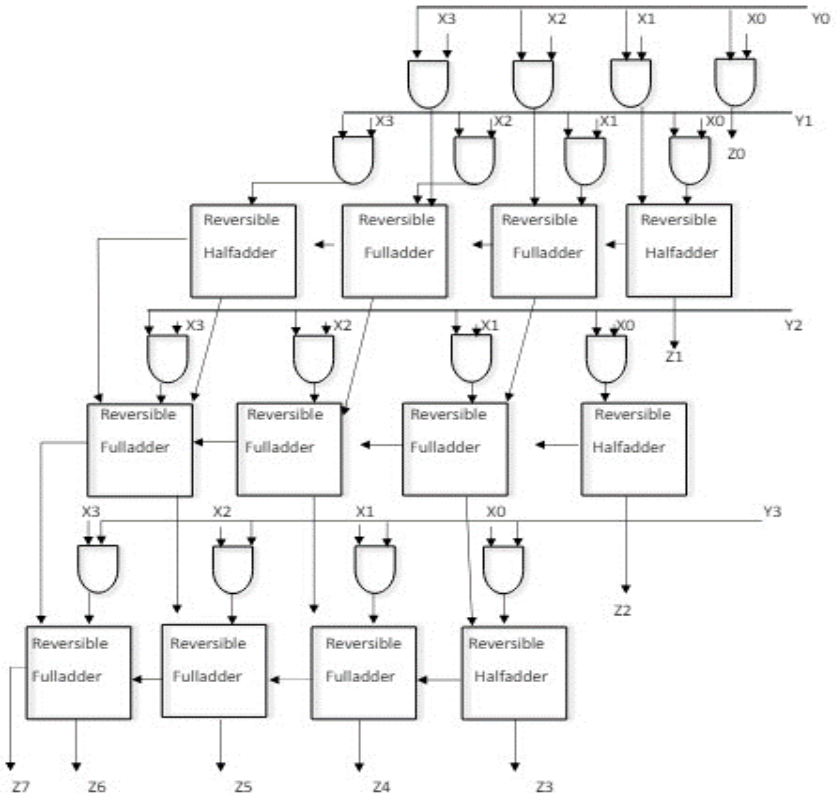

Fig. 3: Architecture of proposed multiplier using Reversible logic

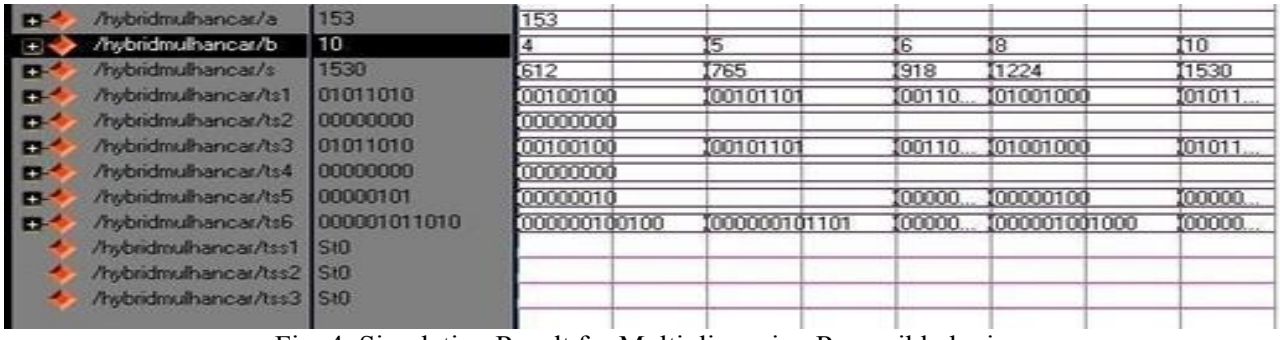

Fig. 4: Simulation Result for Multiplier using Reversible logic.

Table 1. Simulation Result of different Multiplier with Spartan6 FPGA Implementation

S. No.	Name of the Technique	Delay (ns)	No. of LUTs	Power (uW)	ADP	PDP
1	Proposed Multiplier using Reversible logic	12.55	82	54.25	1121.25	820.93
2	Wallace tree multiplier	21.02	116	59.24	2438.32	1245.2
3	Array Multiplier	21.43	84	52.52	1800.12	1125.5