Efficient 32-nm CNTFET-Based 1-Bit Adder: A Fast and Energy-Optimized Design

VENKATA RAO TIRUMALASETTY, K. BABULU, G. APPALA NAIDU
Department of ECE, JNTUGV,
Vizianagaram, Andhra Pradesh,
INDIA

Abstract: - CNTFETs are a shows potential choice for traditional CMOS technology due to their potential for lesser power consumption and superior performance. In the present paper, a new 1-bit hybrid full adder has been deliberated and proposed using both pass transistor (PT) and transmission gate logics (TGL), which utilizes a total of 16 transistors. The combination of PT and TGL can lead to improved power efficiency, reduced delay, and enhanced circuit performance in various VLSI applications. For 0.9 V supply voltage at 32-nm CNTFET technology, the power consumption is 0.0748 μW, which is to be an exceptionally low value with a lesser delay of 7.586 Ps and the power-delay-product (PDP) of 0.5674 aJ. The results obtained from this analysis demonstrate the power efficiency, speed, and overall performance of the proposed full adder design. The combination of 32-nm CNTFET technology, deliberate circuit design choices, and the use of specific logic elements (CMOS inverters and strong transmission gates) contributes to the reported characteristics. Using a 0.9 V supply voltage and 32-nm Stanford CNTFET Model technology, the suggested 1-bit adder circuit's concert was investigated using the Mentor Graphics Tool. Finally, using the proposed 1-bit full adder circuit, an N-bit ripple carry adder (N=8, 16 & 32) is implemented and demonstrated. The Simulation results of the 8-bit RCA with a power consumption of 0.373 μW, the delay is 16.852 Ps and the PDP is 6.2857 aJ. These results show that proposed RCA's have better performance compared to the already reported designs in terms of performance, speed, and power economy.

Key-Words: - 1-bit adder, Low Power, Speed, Power Delay Product, NCNTFET & PCNTFET, Pass Transistor & Transmission Gates, Digital Integrated Circuits.

Received: June 29, 2023. Revised: December 15, 2023. Accepted: January 21, 2024. Published: April 9, 2024.

1 Introduction

A Full adder is the fundamental module for the various digital and analog VLSI circuits. Full adder cells are used in many VLSI applications like Application-specific digital signal processing (DSP) Architectures, Microprocessors, Arithmetic Logic Units, Multipliers, and Mobile communication, [1]. It is also used in many other applications such as binary numbers addition, binary numbers subtraction, and as well as address calculations, [2]. The presentation and proficiency of number arithmetic circuits fundamentally influence the general usefulness and capacities of digital systems, [3]. To improve the performance of the 1-bit adder cell, there is tremendous research going on in terms of circuit designing, [4]; logic style is to be used as and geometrical representation of transistor, [5].

CNTFET is a promising device that replaces the silicon-based transistors. Since, it has several advantages like low power consumption, small in size, operation at lower supply voltages, etc. CNTFET's promising advances are forefront of nanotechnology. Owing to the incessant scaling of the MOS transistor has encountered significant short-channel effects. CNTFET can do high productivity and is utilized in a large number of uses in many surges of science and innovation, [6]. CNTFETs are the alternative devices to the silicon-based transistors. These are supposed to be the sub-atomic components that stay away from the essential silicon limitation in ballistic transport. Its structure depends upon the threshold voltage of the device. That indicates threshold voltage changes; the device structure will be changed i.e. geometrical structure, [7].

CNTFET had four terminals like MOS transistor terminals, in which carbon nanotube acts as a conducting path i.e. channel between source and drain terminals. As indicated by the capability of CNTFETs can be categorized into two classifications, Schottky Barrier CNTFET (SB-CNTFET) and MOS transistor-based CNTFET (MOS-CNTFET) are shown in Figure 1(a) and Figure (b).

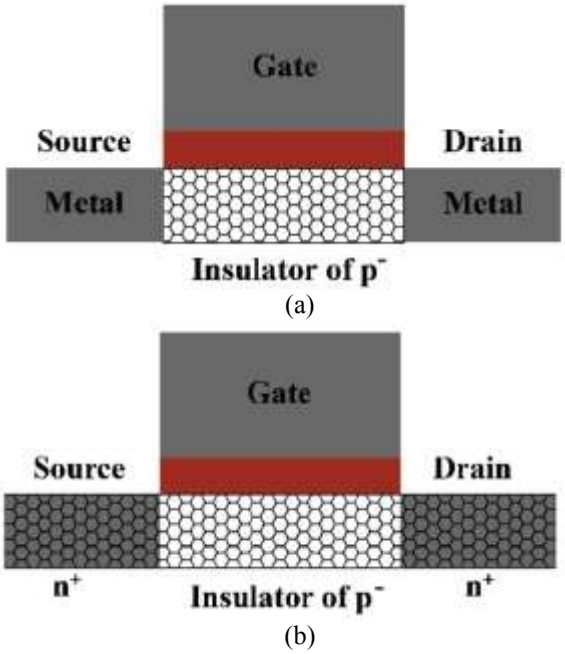

Fig. 1: (a) SB-CNTFET (b) MOS-CNTFET

The basic operation of the SB-CNTFET is based on the charge carriers flowing through the barriers of the device contacts. In the case of MOS-CNTFET, charge carriers flow through the conducting channel. The conducting channel is the carbon nanotube. Depending upon the type of charge carrier flowing through the channel, there are two types of MOS-CNTFETs. If the majority are electrons then the device is N-CNTFET and if the majority are holes then the device is P-CNTFET, [8]. The CNTFET parameters Diameter of Carbon nanotube (D_{CNT}) and threshold voltage are calculated using the mathematical equations (1) and (2) shown below, [9].

$$D_{CNT} = \frac{a \times \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\Pi} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (1)$$

$$V_{th} \approx \frac{E_g}{2.e} = \frac{\sqrt{3}}{3} \frac{a.V_\Pi}{e.D_{CNT}} \approx \frac{0.43}{D_{CNT}} \quad (2)$$

Where the *n1* and *n2* are chiral numbers, Eg is the band gap of CNTFET, and D_{CNT} is the diameter of nanotubes. The CNTFET transistor is based on Stanford CNTFET 32 nm model technology and the parameters are indicated in Table 1.

Table. 1 CNTFET parameters

CNFET Parameter	Value	Brief Description
Supply	0.9V	Gate Supply Voltage
$L_{channel}$	32 nm	Channel Length in terms of nano meter
L_{ss} / L_{dd}	32 nm	Fermi level of doped Carbon Nano Tube source/drain region
t_{ox}	4 nm	The thickness of dielectric material
K	16	Dielectric constant
E_{fi}	6 eV	Fermi level of the doped source/drain
C_{sub}	20 pf/m	Capacitance between channel to substrate
Pitch	20 nm	The distance between the centers of two neighboring CNTs within the same device
Tubes	3	Number of CNTs
n_1,n_2	19,0	Chirality Vector

2 Existing Full Adder Designs

The choice of a Full Adder design depends on the particular desires and constraints of the target application. The existing full adder implementations using different logics are as follows

CMOS 1-bit Adder: CMOS consists of complementary devices both P-CNTFET & N-CNTFET are connected. P-CNTFET is connected as a pull up network, which is connected to supply voltage (V_{dd}), and in the case of N-CNTFET connected as a pull down network, which is connected to ground (V_{ss}). For implementation 1-bit adder using CMOS logic, it requires 28 transistors, [10]. CMOS-based adder has low power consumption, robust to voltage scaling, and high noise margin. It requires a larger number of transistors for designing a 1-bit adder i.e. complexity of the circuit increases.

CPL-based 1-bit Full Adder: CPL based 1-bit adder requires 32 transistors for implementing 1-bit full adder, [11]. CPL full adders offer low power consumption and are suitable for low-voltage applications. However, they may have limited noise tolerance and require careful sizing of transistors to ensure proper operation.

TG-CMOS based 1-bit Full Adder: TGCMOS (Transmission Gate CMOS) full adders combine the advantages of transmission gate logic and Complementary MOS logic, [12]. It requires 20 transistors to implement 1-bit full adder.

TFA based 1-bit Full Adder: Transmission Function Adder (TFA) requires 20 transistors for implementing a 1-bit cell, [13]. For higher order adder implementations that can be done using TFA, the output voltage swing is reduced.

The above logic CMOS, CPL, and TFA-based adders utilize single logic for the entire circuit. The logic style uses two different logic for implementation of a 1-bit adder circuit known as hybrid logic, [14]. The hybrid logics are

1-bit adder (10T): In 10 T-based added circuit was designed using pass transistor and CMOS based logics, as presented in [15], having only used ten transistors. Due to the PT logic, present a threshold voltage drop exists and the output of the adder circuit is affected.

1-bit adder cell (16T): For 16T based added circuit was implemented using hybrid logic i.e. pass transistor (PT) and transmission gate (TG) based logics, as depicted in [16], having only used sixteen transistors only. Due to the PT logic, there is a threshold voltage drop that exists and the output voltage swing is reduced.

1-bit Adder Cells (14T & 16T): In this two different adder circuits are implemented, which utilise 14 & 16 transistors. There is a reduction in the output voltage swing, when implementing higher-order adder structures, [17].

1-bit Adder Cell (18T): In 18 transistor adder circuit was designed using the hybrid logic and depicted in [18].

A new CNTFET-based 1-bit adder circuit is presented in references [19] and [20] respectively. These designs combine different logic styles to achieve improved performance.

Hybrid 1-bit Adder Cell: The hybrid adder circuit utilizes 26 transistors for its sum and carries generation as presented in [21]. The adder cell in this paper had better performance, when contrast to the already reported adder circuits.

A novel CNTFET based 1-bit adder circuit was presented in reference [22] and has only 20 transistors for the implementation of adder circuit. Another CNTFET-based 1-bit adder circuit was presented in reference [23]: which utilizes 24 transistors for the implementation of the adder circuit

While hybrid logic adders, such as the ones mentioned previously, can offer excellent performance as 1-bit cells, their driving abilities may be limited. As the number of stages or chains in a cascaded configuration increases, the performance of these adders can degrade significantly. The poor driving capacity issue arises due to increased load capacitance and propagation delays in cascaded structures.

In this paper, we present an adder cell that utilizes PT and TG logics that offer low power consumption, lower delay, and low Power-Delay Product (PDP). This is achieved by utilizing a combination of consolidation CMOS inverter and robust transmission gates. To achieve low power consumption, the cell schematic is designed with minimum transistors and optimized transistor-transistor connections. The goal is to minimize power dissipation while ensuring the circuit's voltage and device scaling robustness.

The remaining structure of the paper is ordered as follows: The proposed 1-bit adder cell discussed in section 3; consists of three modules XOR-XNOR, sum, and carry circuits. The proposed adder cell was simulated using Mentor Graphics Tool and using 32 nm Stanford CNTFET Model technologies; these results are discussed in section 4. Using the proposed 1-bit adder cell; N-bit ripple carry adder (N=8, 16 & 32) was implemented and these results are presented in section 5. Finally, the conclusion was depicted in section 6.

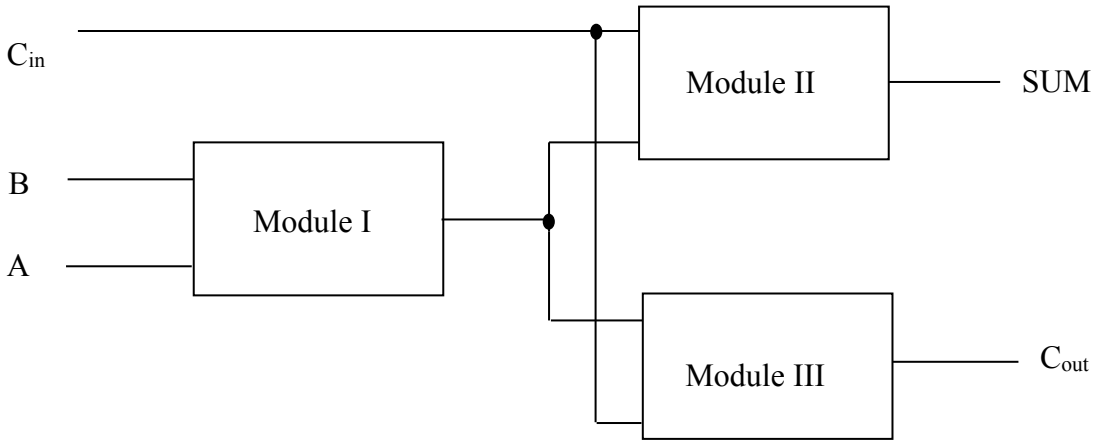

Fig. 2: Block diagram of Proposed 1-bit Full adder

3 Implementation of Proposed 1-Bit Adder Cell

A full adder is a basic component for the implementation of digital circuits; having three inputs and two outputs. The inputs are typically labeled A, B, and Cin, representing the two binary numbers to be added (A & B) and the input carry (Cin). The outputs are designated as Sum and Cout and the relationships between the inputs (A, B, and Cin) and the outputs (Sum and Cout) are

$$Sum = ABCin + \overline{A}\overline{B}Cin + \overline{A}B\overline{Cin} + A\overline{B}\overline{Cin} \quad (3)$$

$$Cout = AB + BCin + ACin \quad (4)$$

The basic block diagram of the proposed 1-bit full adder as shown in Figure 2 consists of three modules employed to execute the addition operation. Module I acts as an XOR-XNOR circuit; The XNOR output is considered as the inverting of the XOR output. Module II is responsible for generating the Sum output (SUM). It takes the output from Module I and the Cin, as inputs. Module III focuses on implementing the output carry (C_{out}) using the PT and TG logics.

Module I represented the XOR and XNOR combined circuit; The XNOR output is considered as the inverting of the XOR output. It consists of a current source configuration, in which P-CNTFET is constantly ON state irrespective of functional input voltage conditions. And the N-CNTFET ON/OFF condition depends upon the applied input (A) value. The current source configurations with output-driving transistors are shown in Figure 3.

The current source is a common gate design using the P-CNTFET with its gate terminal connected to the V_{DD}. Due to this P-CNTFET is constantly ON state and N- CNTFET transistor works as a pull-down arrangement. The current source structure acts as an inverter; which has more voltage gain, compared to the dynamic load structures.

The projected 1-bit full adder cell circuit is presented in Figure 3; utilizes 16 transistors only for designing 1-bit adder cell. The proposed circuit was implemented using XOR-XNOR circuit, sum, and carry circuits based on the basic block diagram of the proposed adder structure shown in Figure. 2.

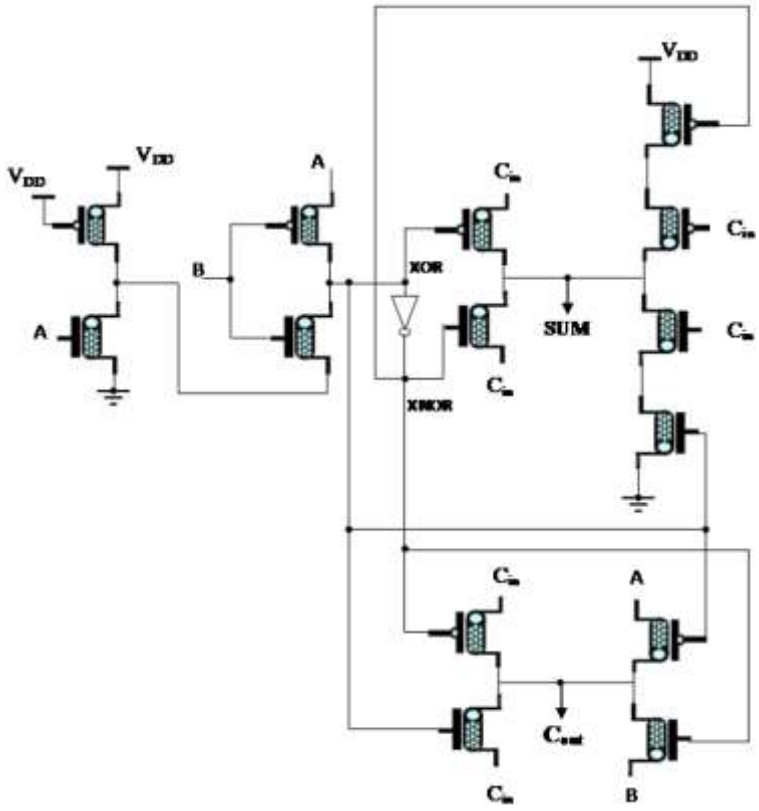

Fig. 3: Proposed 1-bit full adder cell circuit using 16 CNTFETs

The proposed sum circuit utilizes 6 transistors only; in which two P-CNTFET transistors and the N-CNTFET transistors are connected in a series manner for implementing the sum output. The P-CNTFET transistor and the N-CNTFET transistor perform the operation of XNOR output functionality to implement the complete sum output function. Due to use of transmission gates; there is no output voltage swing reduction in sum and carry outputs. Since the transmission gate has stronger 1's and stronger 0's; when it is ON condition.

Since both P-CNTFET / N- CNTFET transistors are connected in a series manner and utilization strong transmission gates; the proposed 1-bit adder circuit provides better voltage swing at the output and it is efficient in terms of power, speed, and PDP.

4 Simulation Results

The proposed adder circuit and the other conventional adder circuits in the paper were simulated using the Mentor Graphics Tool and using 32 nm Stanford CNTFET Model technologies, [24], at room temperature. The operating supply voltage of the proposed adder circuit and the other conventional adders is V_{DD}=0.9 V. The parameters used for the simulation are threshold voltage (Vth) of 0.289 V and chirality vector (19, 0). The threshold voltage is calculated using the equation (2).

The threshold voltage is directly depends upon the substrate biasing voltage, oxide layer thickness, and doping concentration. If any one of the parameters changes that directly affects the threshold voltage of the device. The proposed 1-bit adder and other conventional adder cells simulated results are enumerated in Table 2. The proposed adder circuit outperforms in terms of power consumption, delay, and PDP.

The power consumption of the proposed 1-bit full adder circuit is 0.0748 µW, the delay is 7.586 Ps, which was extremely very low value compared to other reported designs and the power delay product (PDP) is 0.5674 aJ.

In Table 2, CMOS, HCTG, CNTFET based adders, CNTFET full adders, HMTFA, and CNTAFS based adders have extremely low power consumption after the proposed one. In CMOS-based adder consists of complementry transistors, depending upon the applied input combinations one of the transistors is in ON condition and the other will be in OFF condition. Due to this CMOS-based adder having low power consumption. CNTFET based adder utilizing the tranmission gates for designing a 1-bit full adder cell. Transmission gates provides the full voltage swing without any threshold voltage drop problems.

In contrast to the delay of the adder circuits, CNTFET-based adder and CNTAFS adder have lower delay values. Since these logics utilise the hybrid logics i.e. combination of two different logics.

Table 2. Simulation Results comparisons of the proposed & different implementations of 1-bit full adder cells with V_{dd} = 0.9 V, V_{th}=0.289 V and chirality vector (19, 0) at 32-nm CNTFET model technology

Design	Power(µW)	Delay (Ps)	PDP (aJ)	Transistor Count
CMOS [10]	0.3334	15.674	5.2257	28
CPL [11]	1.3965	14.780	20.6402	32
TGA [12]	0.4954	13.241	6.5595	20
TFA [13]	0.3584	16.253	5.8250	16
HCTG [16]	0.2847	15.421	4.3903	16
Hybrid Adder [17]	0.4528	16.042	7.2638	14
CNTFET based Adder [19]	0.251	10.895	2.7346	20
CNTFET Full Adder [20]	0.362	12.685	4.5919	20
HMTFA [22]	0.1216	16.909	2.0561	20
CNTAFS [23]	1.3854	8.475	11.7412	24
Proposed Full Adder	**0.0748**	**7.586**	**0.5674**	**16**

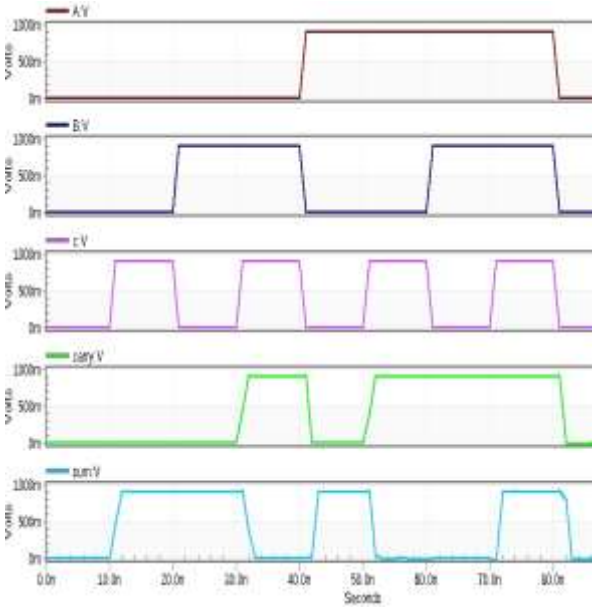

Fig. 4: Simulated input & output waveforms of proposed 1-bit Full Adder cell circuit

The simulated input and output waveforms of the proposed 1-bit adder cell are presented in Figure 4. The inputs (A, B & C) applied all possible test patterns for getting the sum and carry output waveforms i.e. 000 to 111.

5 N-bit RCA implementation

An N-bit parallel adder i.e. ripple carry adder (Nb-RCA) is designed and implemented based on the proposed 1-bit adder. The N value indicates the number of bits i.e. N=8, 16 & 32. The 1-bit full adder cell considered can now be used as the initial structure block of an 8-bit RCA as shown in Figure 5.

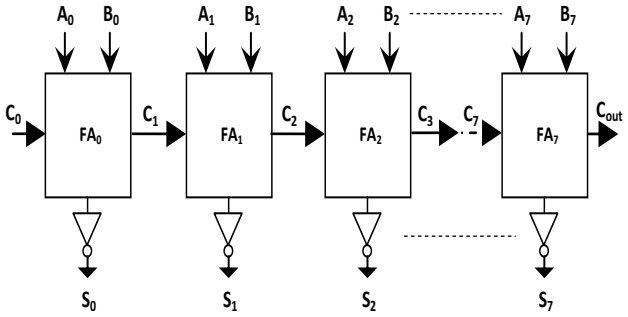

Fig. 5: 8-Bit Ripple Carry Adder implementation using proposed 1-bit full adder

In RCA, the carry signal is propagating from one full adder to another full adder i.e. rippling of the carry signal [25]. For the proposed 8b-RCA, the delay, power consumption, and PDP were noted as 16.852 ps, 0.373 µW & 6.2857 aJ. These extensive results signify that the proposed adder design, when used in the 8b-RCA, 16b-RCA, and 32b-RCAs outperforms the already reported designs in terms of delay, power consumption, and PDP as shown in Table 3.

In the implementation of higher-order ripple carry adder, TGA, TFA, and HCTG based RCA's are failed. That indicates there is a reduction in the output voltage swing in the waveforms. The output voltage swing of sum and carry signals nearly vary from 0.3 V to 0.6 V out of 0.9V.

F*- Failed

The PDP of the projected 8-bit; 16-bit & 32-bit RCAs are 6.2857 aJ, 21.149 aJ and 115.818 aJ. These values show that the proposed RCA is better in energy efficiency.

6 Conclusion

In the present research work, a novel hybrid full-adder circuit has been proposed using both pass transistor and transmission gate logics, utilizing a total of 16 transistors. The simulation analysis was conducted using 32-nm CNTFET technology at 0.9 V single-ended supply voltage using the Mentor Graphics Schematic Design Composer tool. The simulation results show that proposed hybrid full adder cell had a better concert in terms of power, speed (delay) and PDP.

Hence, the proposed adder circuit can be used in many efficient VLSI applications such as ripple carry adders, multipliers, ALUs etc.

Table 3. Performance comparisons of the proposed and other different implementations of 8-bit, 16-bit and 32-bit ripple carry adders with V DD = 0.9 V at 32-nm CNTFET technology

Design	8-Bit RCA			16-Bit RCA			32-Bit RCA		
	Power (µW)	Delay (Ps)	PDP (aJ)	Power (µW)	Delay (Ps)	PDP (aJ)	Power (µW)	Delay (Ps)	PDP (aJ)
CMOS [10]	0.587	38.245	22.449	0.958	64.874	62.149	1.837	113.428	208.367
CPL [11]	3.567	33.428	119.237	5.847	44.592	260.729	9.813	82.629	810.838
TGA [12]	2.895	31.257	90.489	4.587	59.587	273.325	F*	F*	F*
TFA [13]	2.567	44.872	115.186	5.254	83.743	439.985	F*	F*	F*
HCTG [16]	3.287	62.334	204.891	6.189	107.581	665.818	F*	F*	F*
Hybrid Adder [17]	0.487	46.547	22.668	0.984	89.285	87.856	1.768	192.438	340.230
CNTFET based Adder [19]	2.954	47.824	141.272	6.176	92.573	571.730	9.258	171.583	1588.51
CNTFET Full Adder [20]	3.682	24.513	90.256	5.874	46.382	272.447	11.538	105.856	1221.366
HMTFA [22]	0.4867	45.875	22.327	0.754	72.452	54.628	1.357	137.824	187.027
CNTAFS [23]	3.413	28.148	96.069	6.861	53.486	366.967	10.864	97.154	1055.48
Proposed Full Adder	**0.373**	**16.852**	**6.2857**	**0.597**	**35.426**	**21.149**	**1.574**	**73.582**	**115.818**

References:

[1] M. Hasan, M. J. Hossein, M. Hossain, H. U. Zaman, and S. Islam, Design of a scalable low-power 1-Bit hybrid full adder for fast computation, *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 67, no. 8, Aug. 2020, pp. 1464–1468.

[2] A. Kanojia, S. Agrawal and R. Lorenzo, Design Implementation of a Low-Power 16T 1-bit Hybrid Full Adder, *2021 International Conference on Control, Automation, Power and Signal Processing (CAPS)*, India, 2021, pp. 1-5.

[3] A. Misra, S. Birla, N. Singh, and S. K. Dargar, Highperformance 10-transistor adder cell for low-power applications, *IETE Journal of Research*, March 2022 pp. 1-19.

[4] Jiang Y, Klumperink E, Gao X, Ru Z, Zee RVD, Nauta B, Flip-flops for accurate multiphase clocking: transmission gate versus current mode logic. *IEEE Trans Circuits Syst II Express Briefs* 60(7), 2013, pp. 422–426.

[5] Rafiee, Mahmood, Nabiollah Shiri, and Ayoub Sadeghi, High-performance 1-bit full adder with excellent driving capability for multistage structures, *IEEE Embedded Systems Letters*,Vol. 14, no.1, March 2022, pp.47-50.

[6] Xu., Qlu C, Zhao C, Zhang Z, Peng L, Insight ballisticity of room temperature carrier transport in carbon nanotube field effect transistors. *IEEE Trans. Electron Devices* 66(8), 2019, pp. 3535-3540.

[7] Oblte F, Ijeomah G, and Bassi JS, Carbon nanotube field effect transistors: Toward future nanoscale electronics. *International Journal of Computer Applications* (41), 2013, pp. 149-164.

[8] J. Deng and H. S. P. Wong, A compact SPICE model for carbon-nanotube field-effect transistors including non-idealities and its application-Part II: Full device model and circuit performance benchmarking. *IEEE Trans. Electron Devices*, vol. 54, no. 12, 2007 pp. 3195–3205.

[9] P.L. McEuen, M.S. Fuhrer, H. Park, Single-walled carbon nanotube electronics, *IEEE Trans. Nanotechnol.* 99, 2002, pp. 78–85.

[10] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A System Perspective*, MA, USA: Addison-Wesley, 2015.

[11] R. Zimmermann and W. Fichtner, Low-power logic styles: CMOS versus pass-transistor logic. *IEEE Journal Solid-State Circuit*, vol. 32, 1997, pp.1079-1090.

[12] Ilham Hassoune, Denis Flandre, Ian O'Connor and Jean-Didier Legat, ULPFA: A New Efficient Design of a Power-Aware Full adder *IEEE Transactions on Circuits and Systems*-I: Regular papers, Vol. 57, No. 8, August-2010, p.2066-2074.

[13] Shams AM, Darwish IK, Bayoumi MA, Performance analysis of low-power full adder cells. *IEEE Trans Very Larg Scale Integr (VLSI) Syst* 10(1)2002, pp. 20–29.

[14] Alioto M, Cataldo GD, Palumbo G, Mixed full adder topologies for high-performance low-power arithmetic circuits. *Microelectron J* 38(1), 2007, pp. 130–139.

[15] Dokania V, Verma R, Guduri M, Islam A, Design of 10T full adder cell for ultralow-power applications. *Ain Shams Eng J* 9(4), 2018, pp. 2363–2372.

[16] Shams AM, Bayoumi MA, A novel high-performance CMOS 1-bit full-adder cell. *IEEE Transact Circuits Syst II Anal Dig Signal Process* 47(5), 2000, pp.478–481.

[17] Venkata Rao Tirumalasetty & Madhusudhan Reddy Machupalli, Design and analysis of low power high-speed 1-bit full adder cells for VLSI applications, *International Journal of Electronics*, vol. 106:4, 2019, pp.521-536.

[18] Amini-Valashani M, Ayat M, Mirzakuchaki S, Design and analysis of a novel low-power energy-efficient 18T hybrid full adder. *Microelectron J*, 2018, 74, pp. 49–59.

[19] N. Talebipour, P. Keshavarzian, CNTFET-based design of multi-bit adder circuits, *Int. J. Electron.* 104, 2017, pp. 805–820.

[20] Y.S. Mehrabani, R.F. Mirzaee, M. Eshghi, A novel low-energy CNFET-based full adder cell using pass-transistor logic, *Int. J. High Perform. Syst. Archit.* 5, 2015, pp. 193–201.

[21] S. Goel., A. Kumar, and M. Bayoumi, Design of robust, energy-efficient full adders for deep-sub micrometer design using hybrid-CMOS logic style, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, Dec. 2006, pp. 1309–1320.

[22] M. Maleknejad, S. Mohammadi, K. Navi, H. R. Naji, and M. Hosseinzadeh, A CNFET-based hybrid multi-threshold 1-bit full adder design for energy efficient low power applications, *International Journal of Electronics*, June 2018, pp. 1753-1768,

[23] H.T. Tari, A.D. Zarandi, M.R. Reshadinezhad, Design of a high performance CNTFET-based full adder cell applicable in: Carry ripple, carry select and carry skip adders.

Microelectronic Engineering 215, 2019, pp. 1–8.

[24] Stanford CNTFET Model, [Online]. https://nano.stanford.edu/downloads/stanford-cnfet-model (Accessed Date: February 20, 2024).

[25] Venkata Rao Tirumalasetty, P Balakrishna, M Chaitanya Suman, N Prasad, K Prathyusha, M Suman, Low Static Power Consumption and High Performance 16-Bit Ripple Carry Adder Implementation by Using BBL-PT Logic style, *International Journal of Applied Engineering Research*, Vol. 9, Number 23, 2014, pp. 22727-22741.

Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

- Venkata Rao Tirumalasetty: Conceptualizing, investigation, theory, modelling, writing original draft.
- K. Babulu: Simulation results checking, review and editing.
- G. Appala Naidu: Simulation results checking, review and editing.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

No funding was received for conducting this study.

Conflict of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article.