Single-Source based Switched-Capacitor Seven-Level Inverter

LAKSHMI PRASANNA[1], T. R. JYOTHSNA[1], KURRA VENKETESWARA RAO[2],
VEMANA.U. P. LAVANAYA[2], P. VINOD[1]
[1]Department of Electrical Engineering,
Andhra University,
Visakhapatnam,
INDIA

[2]Department of Electrical and Electronics Engineering,
Aditya University,
Surampalem,
INDIA

Abstract: - In this article, a novel seven-level inverter that performs on a single DC source and is suitable for solar and wind applications is described. By integrating floating capacitors (FC) using a switched-capacitor method, the desired outcome is produced. Due to its sensorless capacitor voltage balancing capability, which minimizes control concerns when generating a tripolar staircase pattern, this arrangement has gained recognition. Sustainable performance that prevents accidental capacitor overvoltage is another benefit. To regulate the topology's operation, a phase disposition pulse-width modulation (PD-PWM) technique has been used. Additionally, fewer semiconductor devices are used in the suggested topology. To demonstrate the positive aspects of the suggested structure regarding reducing the number of switches, a thorough comparison of various recently developed 7L inverter designs is given. Under various parametric constraints, the effective implementation of the suggested structure is examined using MATLAB/Simulink. The feasibility of the study and the functionality of the proposed topology are subsequently verified using hardware-in-loop (HIL) experiments.

Key-Words: - Multi-level inverter, self-voltage balancing, single-source, switched capacitor, Total Harmonic Distortion, Total Standing Voltage, OPAL-RT.

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1 Introduction

For industrial and renewable energy conversion applications, multilevel inverters (MLI) are growing in popularity owing to their enhanced waveform compared to two-level inverters. MLIs are attractive due to their minimal total harmonic distortion (THD), low dv/dt stress, switching loss, and extremely similar sinusoidal output voltage evolution. Traditional MLIs are often divided into three types: cascaded H-bridge (CHB), flying capacitor (FC), and neutral point clamped (NPC), [1]. Capacitor voltage imbalance in NPC and FC is one of the drawbacks of these conventional MLIs. Although more recognized DC sources are included, the cascaded bridge MLI draws the interest of traditional inverters. In traditional MLI, higher voltage levels need an increase in the number of switches. There have been several attempts by researchers to develop a large number of reduced switch count (RSC) MLIs to analyze the issues with traditional MLIs. Unlike simple MLI designs, these arrangements use fewer switches and diodes to achieve the same number of levels, [2], [3], [4].

With conventional or RSC MLI, voltage enhancement is not possible. Voltage boosting will be essential in alternative energy conversion processes since solar panels produce a low voltage. In order to achieve a broad range of levels and a notable increase utilizing an isolated source, the researchers created the switched capacitor technique. Higher levels are achieved by energizing the capacitors in parallel with the source and discharging them in series with the source, [5], [6]. The first bridge in [7], is powered by a DC supply, while the other two bridges are connected by two bidirectional switches. The other bridges are configured with switched capacitors. In order to activate these capacitors, interconnected switches are used. The authors proposed a topology that uses

fewer switching devices than the other seven-level inverters that were discussed, [8].

By connecting a buck-boost converter and an inverter with the aid of two capacitors, voltage enhancement is accomplished, [9]. While reducing the maximum load current on the switches, the front side structure of the design can provide a triple boost increase in voltage. Three distinct stages are used to produce a (2N+1) level inverter, [10]. A switched capacitor unit in the middle and an H-bridge inverter at the end come before the front-end configuration with improving capability. A diamond-shaped arrangement is shown, which offers the advantages of triple gain and a decrease in total standing voltage (TSV), [11].

A novel 5L inverter concerning twice boosting is developed and extended to a standardized inverter, [12]. To lessen current stress and keep the capacitor current within an appropriate range, this setup incorporates a quasi-soft charging technique. A few components are used to present a topology in [13]. According to the authors, the structure can regenerate, meaning that in the event that the capacitor overcharges, energy will be abruptly transferred to the source.

In order to achieve seven levels, a configuration that combines a full bridge inverter with two T-type circuits has been proposed [14], yet it requires a higher number of switches. A unique T-type inverter that maximizes capacitor efficiency is described, [15]. Three capacitors are used in a seven-level design that has minimal TSV, [16]. A unique boosting ANPC with surplus TSV for seven-level inverters is published in [17]. The packed U-cell (PUC) has been adapted in [18], to use fewer switches to achieve seven levels at the output. The half-bridge unit with a switched capacitor cell in [19], can be used to produce a seven-level inverter with a minimal number of switches. Combining a DC-link module, a bidirectional switch cell, and an output module, [20], produces a seven-level inverter. 13 semiconductor devices and 3 capacitors are used to create a 13-level inverter in [21], with the use of a switched capacitor approach.

The benefits of the suggested configuration are as follows:

- It achieves output voltage with a 1:3 boosting ability.
- A single DC supply is required.
- Sensors are not required to maintain voltage balance across capacitors.
- It can function with either a leading or trailing power factor; each half-cycle has the same number of energizing and de-energizing modes.

A unique MLI configuration is proposed in this study to lower TSV and switch count. The structure of this work is as follows: A thorough examination of the suggested topology, operating modes, voltage analysis, pulse width modulation method, and capacitor design calculation is provided in Section II. The suggested topology and other existing topologies are contrasted in Section III. The HIL implementation and simulation results for various loading conditions are examined in Section IV. Section V depicts the completion of the work.

2 Proposed Topology

Figure 1 shows the proposed MLI configuration. Eight switches, two capacitors (C_1 and C_2), one diode, and a single DC source make up the circuit layout. Capacitors C_1 and C_2 have respective maximum voltage ratings of V_{dc} and $2V_{dc}$. Two switches (S_4&S_6) out of the eight power semiconductor devices are just IGBTs, while the other switches are IGBTs connected in parallel with a diode. The complimentary devices S_1, S_2, S_7, and S_8 are arranged in such a way that their conductivity at the same time causes the DC voltage source condition to fail. Consequently, these switching configurations must function in complementary mode. The proposed unit's switching modes are listed in Table 1 (Appendix). In Table 1 (Appendix), the switches off state is denoted by 0 and its on position by 1. Every mode in the suggested topology is depicted in Figure 2 (Appendix) together with the switching modes mentioned in Table 1 (Appendix). The conducting path, non-conducting path, and charging path of capacitors are represented by the colours green, red, and black, respectively, in Figure 2 (Appendix).

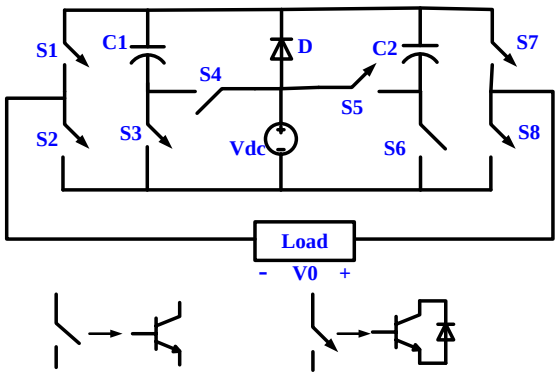


Fig. 1: Proposed Topology

2.1 Operating Modes

Figure 2 (Appendix) illustrates how each operating mode generates an output voltage. In Table 1

(Appendix), the colours yellow, grey, and green stand for the positive, zero, and negative modes, respectively.

State A: To provide $+3V_{dc}$ voltage across the load, the DC source and capacitor C_2 are discharged through the conductivity channel of S_2, S_5, and S_7 for state A listed in Table 1 (Appendix). This mode of operation is seen in Appendix in Figure 2(a); the diode is reverse biased and capacitor C_1 has no effect on operation.

State B: The conductivity path is created by switches S_2, S_4, and S_7 to connect the DC voltage source and capacitor C_1 to the load in order to provide an output voltage of $+2V_{dc}$. This working mode and the charging of capacitor C_2 utilizing a DC voltage source and capacitor C_1 via the conduction of S_4 and S_6 switches are shown in Appendix in Figure 2(b).

State C: With the conductivity of the diode, S_2, and S_7 switches depicted in Appendix in Figure 2(c), a $+1V_{dc}$ level can be produced. Capacitor C_1 is charged by using the S_3 switch, while capacitor C_2 impact remains unchanged.

State D: As seen in Appendix in Figure 2(d), the conduction of switches S_2, S_3, and S_8 produces zero voltage. By using diode forward biasing and switch S_3 conductivity to connect the DC source to C_1, capacitor C_1 is powered to voltage V_{dc}.

State E: Alternating conduction of switches S_1 and S_7, respectively, as shown in Appendix in Figure 2(e), yields zero voltage in a manner similar to state D. The charging of capacitor C_1 occurs in the same manner as described in state D.

State F: As shown in Appendix in Figure 2(f), a diode and switches S_1 and S_8 conductivity are used to connect the DC source to the load to achieve a $-1V_{dc}$ level. Capacitor C_1 is activated to V_{dc} voltage in state E, with no impact from capacitor C_2.

State G: Switches S_1, S_4, and S_8, respectively, are used to discharge capacitor C_1 to load to reach a DC source and $-2V_{dc}$ level, as shown in Appendix in Figure 2(g). Using the connections of C_1, DC source, and switches S_4 and S_6, capacitor C_2 is powered to $2V_{dc}$.

State H: Figure 2(h) in Appendix illustrates how to turn on switches S_1, S_5, and S_8 to connect the DC source and capacitor C_2 to the load to obtain a $-3V_{dc}$ level. C_1 does not take an active part in this manner of operation.

2.2 Voltage Stress Analysis

The voltage stress created by the switching devices is calculated using the maximum voltage of the switches in the event of a turn-off situation. Peak voltage stress is $2V_{dc}$ for switches S_1, S_2, and S_4, V_{dc} for switches S_3, S_6, and diode, and $3V_{dc}$ for switches S_5, S_7, and S_8. Consequently, the TSV (p.u.) for the recommended configuration is 6. Figure 3 shows the voltage stress at each level as a bar chart. Every switch's voltage stress is represented by the different colours.

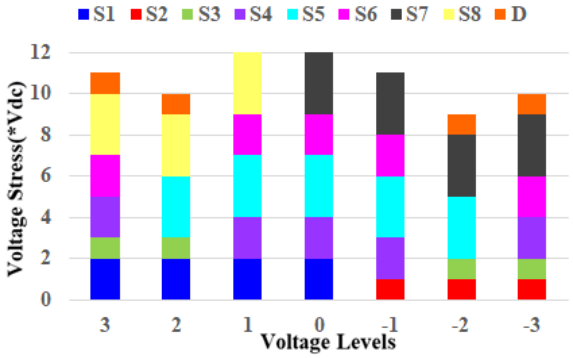


Fig. 3: Bar Chart Representation

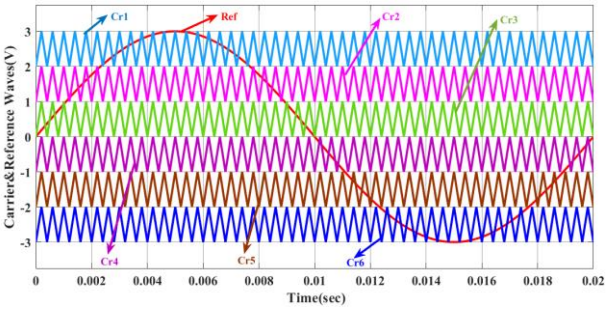


Fig. 4: LSPWM Scheme

2.3 Modulation Scheme

Figure 4 shows the LSPWM method applied to the proposed configuration. Six carriers and a reference wave are needed by this seven-level inverter to supply gate pulses to switches. This modulation technique correlates reference wave and carrier signals to produce gating pulses. Due to the comparison, six pulses are generated. Gate signals are sent to switches (S_1-S_8) by these six pulses using the operating states listed in Table 1 (Appendix).

2.4 Self-Voltage Balancing

Inverters of the switched capacitor kind operate using a series-parallel methodology. The capacitor is connected in series with the DC source to drain it and in parallel to the DC, source to activate it in order to achieve high voltage gain. In State C, Capacitor C_1 is charged to V_{dc}, and in State D or State E respectively, as shown in Table 1 (Appendix). Capacitor C_2 is similarly charged to $2V_{dc}$ in States B and G respectively. Between regular discharging and charging, the capacitor voltages C_1 and C_2 maintain equilibrium at V_{dc} and $2V_{dc}$ respectively, throughout each cycle.

3 Comparison

The proposed structure is compared to other topologies for seven-level operations in Table 2 (Appendix). The comparison variables are TSV (p.u.), cost factor (CF), the number of switches, drivers, diodes, capacitors needed, and DC sources. For all topologies with a DC source count, one is used. [7], requires more switches but has a gain of three. Switch counts drop with the same gain for [8], compared to [7], and just one diode is required. With the same gain as [7], [9], [11], [12], have fewer switches, but there is an imbalance in the voltage of the capacitors. In comparison to other topologies, [14], requires fewer switches, but the gain is half of what is stated for other topologies. In comparison, the suggested architecture shows fewer devices and the best TSV (p.u.) and CF when all factors are taken into account. It illustrates the exquisite higher performance of the suggested topology.

4 Results and Discussions

4.1 Simulation Results

With MATLAB/Simulink, effective execution of the proposed design for seven-level operation is planned. C_1 and C_2 capacitors have source voltages of 100V and self-voltages of 100V and 200V, respectively. In this instance, the resistance and inductance are 100Ω and 100mH, respectively. 1700µF is the capacitance value of both capacitors. 50 Hz is the fundamental frequency at which the suggested inverter operates. The output of the inverter under R-load conditions is shown in Figure 5. The output voltage seems to be correlated with the output current. The performance of the inverter for seven-level operation is shown in Figure 6 under different load conditions. In this instance, the output current is set to null for no load, the same as the voltage for R load, and lagging for RL load. Although C1 and C2's voltages are balanced at V_{dc} and $2V_{dc}$ respectively, load conditions have an impact on the voltage ripples in the capacitors. The output impedance variation is shown in Figure 7 for distinct inductances. Figure 7 illustrates how the current decreases and becomes more lagging as the inductance increases.

The resultant waveforms for modulation index fluctuation (ma) are shown in Figure 8. This arrangement operates as a seven-level system with a peak amplitude of ±3Vdc for modulation index variations of 1, 0.9, and 0.7. However, as the modulation index decreases, the stepped waveform's amplitude breadth decreases. Similarly, with values of 0.6, 0.4, and 0.2, it functions as a five-level inverter, a reduced width five-level inverter, and a three-level inverter, respectively.

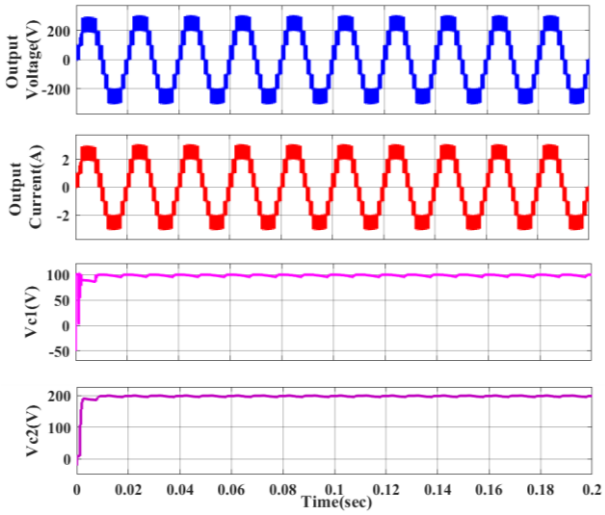


Fig. 5: Resultant waveforms for R-Load

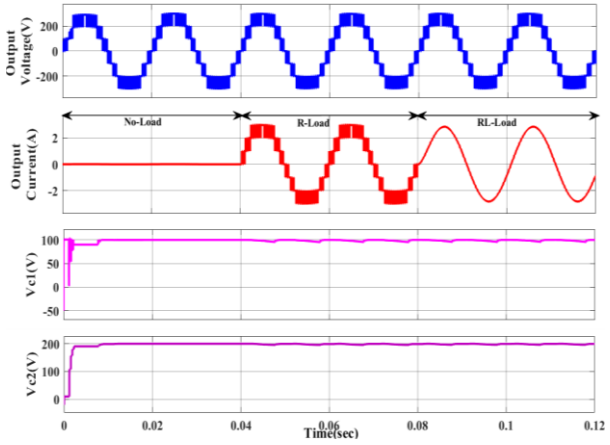


Fig. 6: Resultant Waveforms for Various Load Scenarios

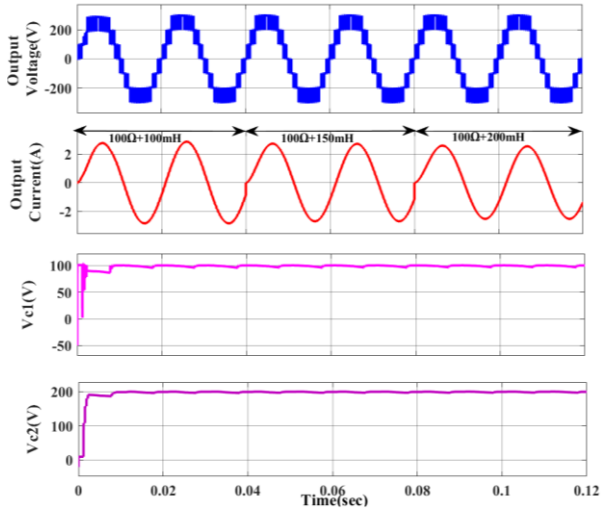


Fig. 7: Resultant Waveforms for Distinct RL-Loads

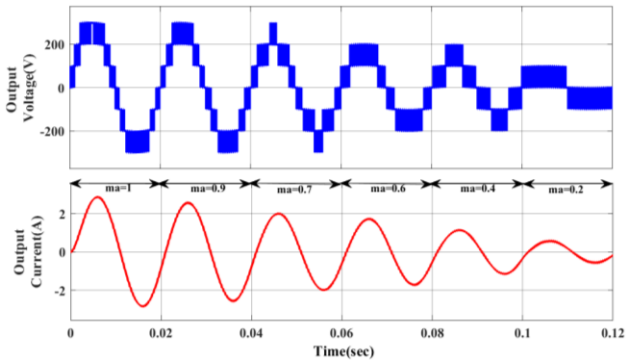


Fig. 8: Resultant Waveforms for variation in modulation index

Figure 9 and Figure 10 represent %THD of output voltage and current assumed load as 100Ω+100mH. %THD of output voltage is 18.43 with a fundamental output voltage of 297.6 volts and %THD of output current is 6.36.

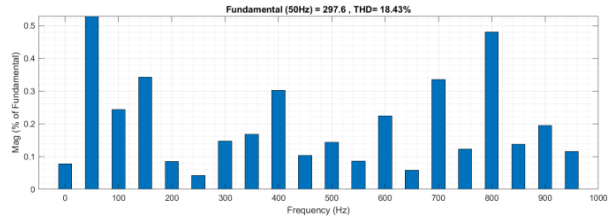


Fig. 9: %THD of voltage

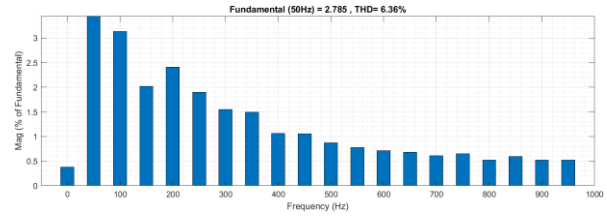


Fig. 10: %THD of current

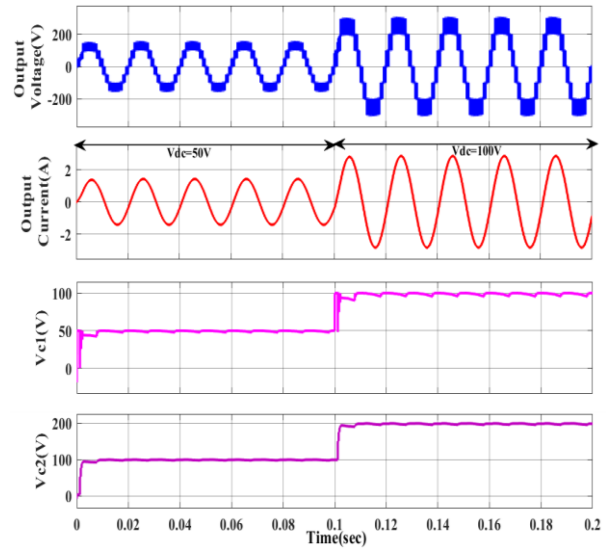


Fig. 11: Resultant Waveforms for regulation of source voltage

Figure 11 shows the output waveforms as well as capacitor voltages for modification of input voltage. Since the source voltage elevates from 50V to 100V, the capacitor voltages C_1 and C_2 unexpectedly rise from 50V to 100V and 100V to 200V respectively. The output waveforms are shown in Figure 12 as the reference frequency changes. According to Figure 12, increasing the reference frequency causes the load inductance to increase. Because of the slow increase in load inductance, load current decreases as reference frequency increases. It implies that high-frequency operating loads can be accommodated by the recommended setup.

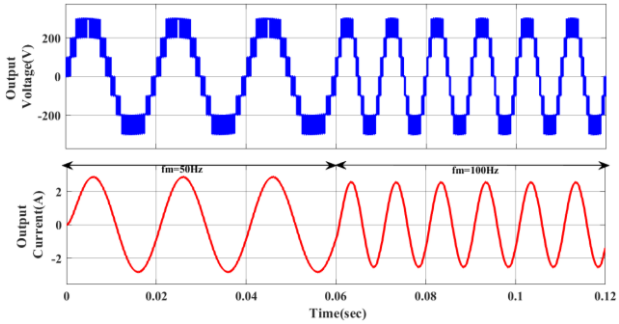


Fig. 12: Resultant Waveforms for variation in reference frequency

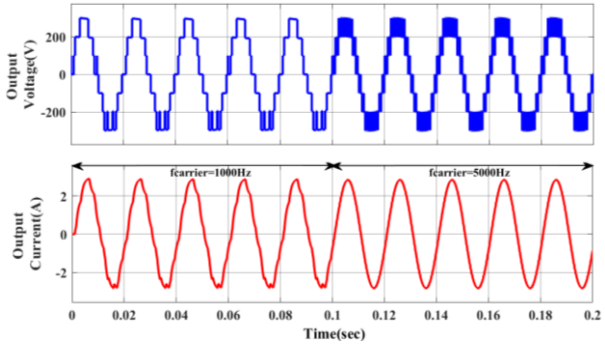


Fig. 13: Resultant Waveforms for variation in carrier frequency

Figure 13 shows waveforms associated with variations in carrier frequency. As the carrier frequency increases, so does the number of pulses for each voltage level. This causes the filter size to be reduced and the harmonics to be moved to a larger number. Switching losses rise with increasing carrier frequency because there are more pulses for each voltage level instance. According to the THD limit and the available filter size, the carrier frequency is then lowered to a predetermined value. In this paper, the carrier frequency is assumed to be 5 kHz under all loading scenarios. The switching patterns of the switching devices are shown in Figure 14. The suggested topology is functioning

under all loading circumstances, according to the simulation results.

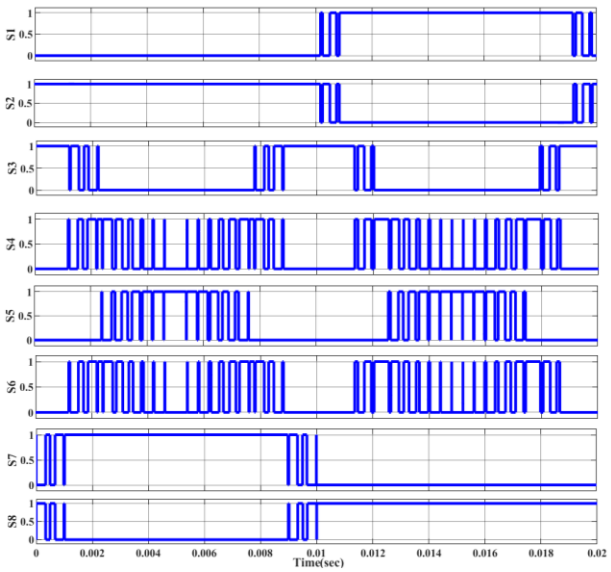


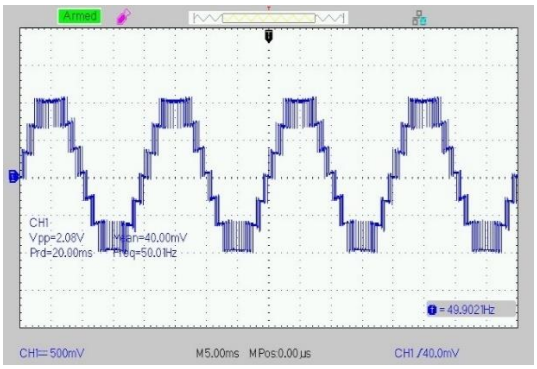
Fig. 14: Switching pulses

4.2 OPAL-RT Results

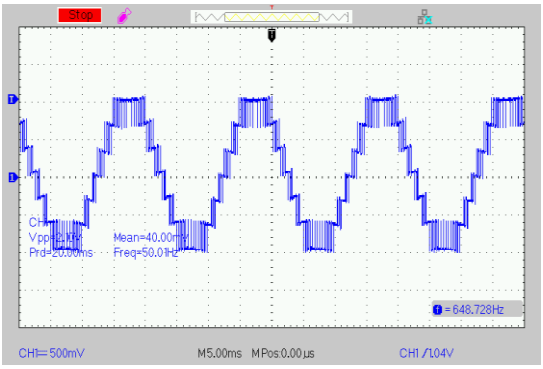
Figure 15 shows the waveforms for loads of 100Ω and 100Ω + 100mH, with a carrier frequency of 5 kHz. The voltage across two capacitors is shown in Figure 15 (c)&(d). It is apparent that the real-time simulated outcomes closely match the simulated results obtained through MATLAB/Simulink. The switching pulses for all the switches are presented in Figure 16. These real-time results show that the proposed configuration performs effectively across capacitors without the need for additional regulation methods.

4.3 Thermal Modelling

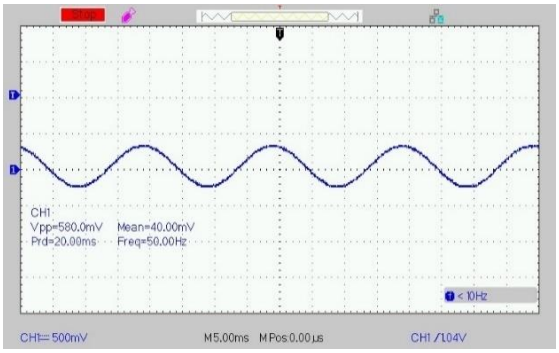
The recommended configuration's power semiconductor components are thermally modelled using PLECS software. The percentage of losses for seven-level operation at loading conditions of 100Ω and 100Ω + 100mH, respectively, are shown in Figure 17(a) and (b). As D and S3 are coupled to the charging circuit, it is evident that their losses are higher than those of other switches. The efficiency is calculated using only R loads and is shown in relation to the output power (0-2000W). Figure 18 illustrates the range of effectiveness, which is 97.6% to 93.4%.



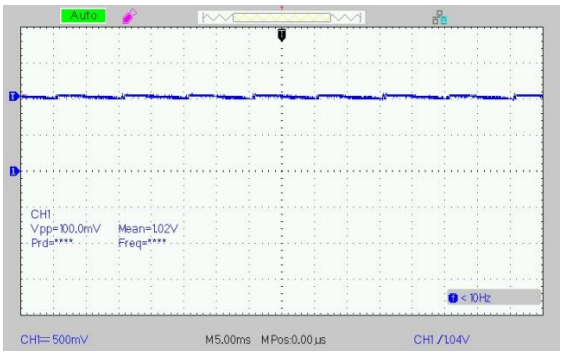
(a) Output Voltage



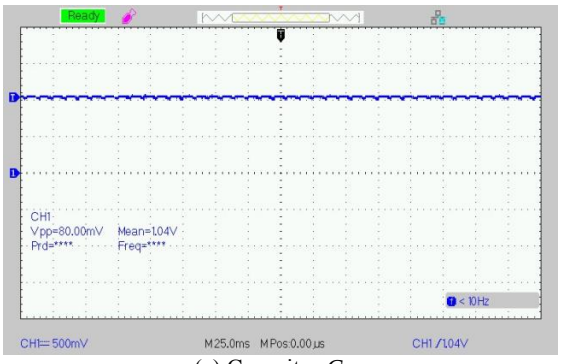
(b) Output Current for R-Load



(c) Output Current for RL-Load

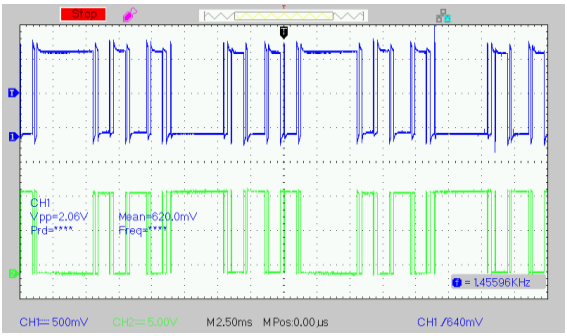


(d) Capacitor C_1

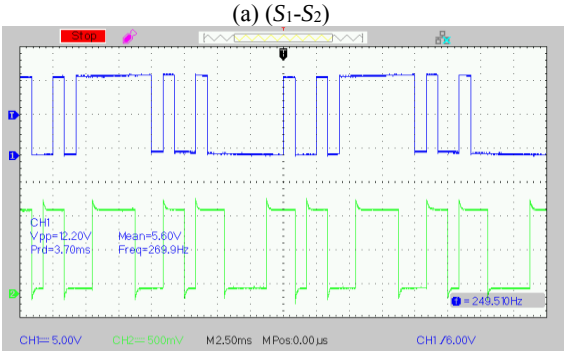


(e) Capacitor C_2

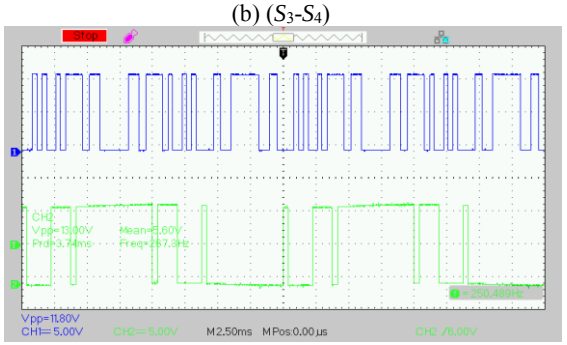
Fig. 15: Resultant Waveforms



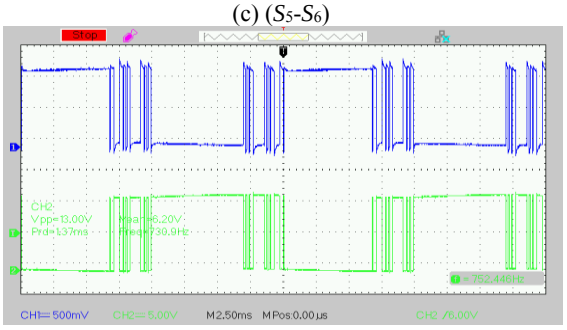
(a) (S_1-S_2)



(b) (S_3-S_4)

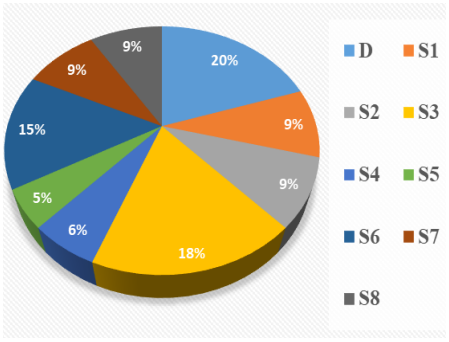


(c) (S_5-S_6)

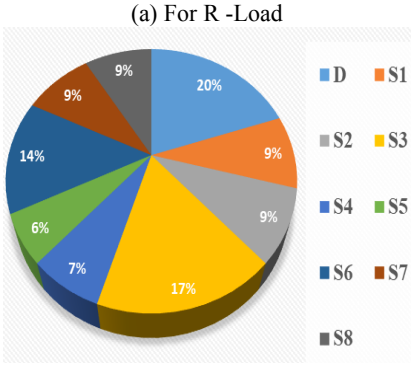


(d) (S_7-S_8)

Fig. 16: Switching Pulses



(a) For R -Load



(b) For RL- Load

Fig. 17: Percentage of losses

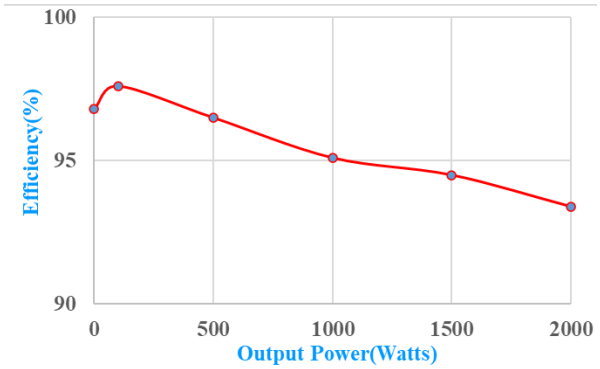


Fig. 18: Efficiency curve

5 Conclusion

This article describes a novel seven-level triple inverter that allows capacitor voltages to self-balance by using a switched capacitor approach. MATLAB/Simulink is used to simulate the suggested layout, taking into account a number of situations, including changes in the carrier frequency, reference frequency, modulation index, load variations, and source voltage fluctuations. According to the simulation results, the recommended configuration can be used under a variety of loading scenarios. The suggested architecture is compared to existing topologies from the literature in order to evaluate its superior qualities. The suggested design uses few components while keeping a respectable TSV, according to the research. Utilizing PLECS

software, which calculates switch losses, the configuration's overall effectiveness is also assessed. Up to 93.4% efficiency is achieved with the suggested design. The efficient operation of the topology is finally verified using Hardware-in-Loop (HIL) testing, and results are given. According to the results, the suggested design produces exquisite outcomes.

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Conflict of Interest

The authors have no conflicts of interest to declare.

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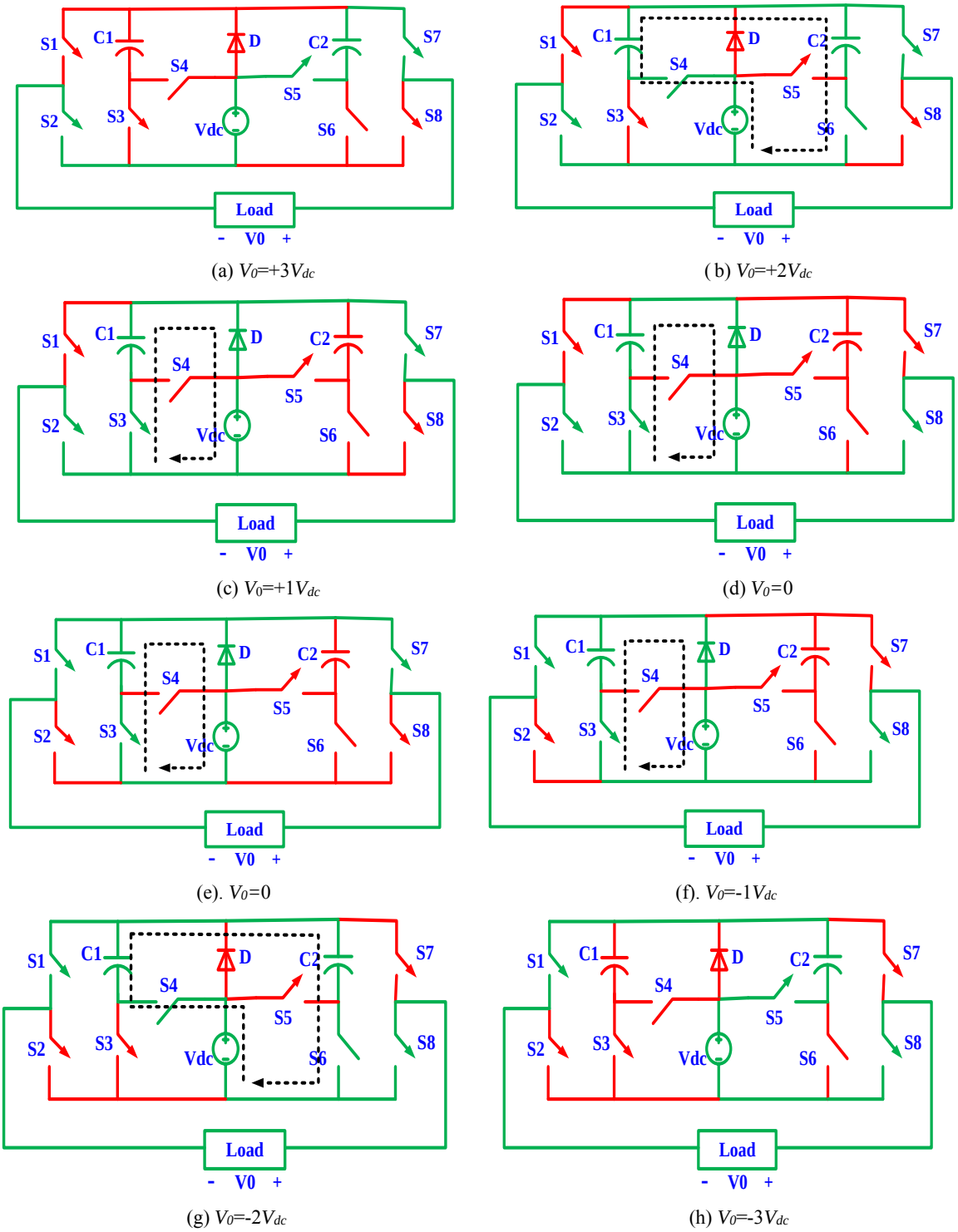
APPENDIX



(a) V_0=+3V_{dc} (b) V_0=+2V_{dc}

(c) V_0=+1V_{dc} (d) V_0=0

(e). V_0=0 (f). V_0=-1V_{dc}

(g) V_0=-2V_{dc} (h) V_0=-3V_{dc}

Fig. 2: Switching modes

Table 1. Operating modes

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_o	C_1	C_2	State
0	1	0	0	1	0	1	0	$+3V_{dc}$	----	D	A
0	1	0	1	0	1	1	0	$+2V_{dc}$	D	C	B
0	1	1	0	0	0	1	0	$+1V_{dc}$	C	----	C
0	1	1	0	0	0	0	1	0	C	----	D
1	0	1	0	0	0	1	0	0	C	----	E
1	0	1	0	0	0	0	1	$-1V_{dc}$	C	----	F
1	0	0	1	0	1	0	1	$-2V_{dc}$	D	C	G
1	0	0	0	1	0	0	1	$-3V_{dc}$	----	D	H

C-charging, D-Discharging, --- No effect

Table 2. Comparison with other topologies

Topology	N_{sw}	$N_{drivers}$	N_{diodes}	N_c	N_{DC}	Gain	TSV (p.u)	CF
[7]	16	16	0	2	1	3	5.3	40.3
[8]	9	9	1	2	1	3	6	28
[9]	12	12	2	3	1	3	7.67	37.6
[11]	12	11	0	2	1	3	5.3	31.3
[12]	11	10	0	3	1	3	6	31
[14]	10	8	0	2	1	1.5	5.3	26.3
Proposed	**8**	**8**	**1**	**2**	**1**	**3**	**6**	**25**