An Efficient Delay Estimation Model for High Speed VLSI Interconnects

M. KAVICHARAN
Dept. of ECE
National Institute of
Technology
Warangal, INDIA

N.S. MURTHY
Dept. of ECE
National Institute of
Technology
Warangal, INDIA

N. BHEEMA RAO
Dept. of ECE
National Institute of
Technology
Warangal, INDIA

Abstract: In this paper a closed-form matrix rational model for the computation of step and finite ramp responses of Resistance Inductance Capacitance (RLC) interconnects in VLSI circuits is presented. This model allows the numerical estimation of delay and overshoot in lossy VLSI interconnects. The proposed method is based on the U-transform, which provides rational function approximation for obtaining passive interconnect model. With the reduced order lossy interconnect transfer function, step and finite ramp responses are obtained and line delay and signal overshoot are estimated. The estimated delay and overshoot values are compared with the Euder method, Pade method and HSPICE W- element model. The 50% delay results are in good agreement with those of HSPICE within 0.5% error while the overshoot error is within 1% for a 2 mm long interconnect. For global lines of length more than 5 mm in SOC (system on chip) applications, the proposed method is found to be nearly four times more accurate than existing methods.

Keywords: Delay; matrix rational model; ramp input; RLC interconnects; transient analysis; transfer function; Uapproximation.

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1. Introduction

As the physical dimensions in VLSI technologies scale down, interconnect delay dominates the gate delay in determining circuit performance [1]. In deep submicron VLSI circuits it is necessary to have computationally economical and accurate interconnect delay models. Thus for the design of complex circuits, more accurate analytic models are needed to predict the interconnect delay accurately.

Originally VLSI interconnects were modeled as RC lines and single pole Elmore-based models [2]–[3] because of long channel device delay dominance over negligible interconnect delay. However for high speed interconnects, inductance effects are becoming progressively important and can no longer be ignored. Under these circumstances, the Elmore model fails since it does not consider the inductance effects [4]. It is necessary to use a second-order model, which includes the effect of inductance. Kahng et al. considered equivalent Elmore delay model based on the Resistance Inductance and Capacitance (RLC) of the interconnects [4] and [5]. Ismail et al. [6] proposed two pole model to capture far end time domain solution for single line interconnect.

A simplified voltage transfer function obtained using Taylor series approximation for transient analysis [7]-[8] has less accuracy in delay calculation. Nakhla et al.[9] use modified nodal analysis (MNA) for obtaining far end and near end responses of interconnects. Roy [10] extended [9] for obtaining more accurate far end responses of coupled RLC interconnects using delay algebraic equations.

A matrix rational-approximation model for SPICE analysis of high-speed interconnects is presented in [11]-[12], however, the approximations made to derive the models contributed to inaccuracy. This has been extended using Pade approximation model [13] to estimate the delay of interconnects. All the above models still suffer from various inaccuracies and need improvement for accurate delay estimations.

In this paper, we present an improved analytic delay model by extending the concepts developed in [11]-[13] for on-chip RLC interconnects. The accuracy of Euder approximation method [16] has been improved by using fourth order MacLaurin series for RLC interconnects and compared with Pade method, proposed method and HSPICE. The proposed model is based on U-transform [14]-[15], which is simple in structure and easier to implement. For a given number of terms used in the transform, the U-approximant requires less algebraic manipulations than the Pade scheme and thus computationally less expensive. This U-transform is used to solve the Telegraphers equation solution for the first time.

The remainder of the paper is organized as follows. Section II briefly describes the mathematical analysis to determine the linear transfer function of RLC interconnect to find the transient analysis. Section III develops the proposed U-model for single RLC line. For validation of the proposed model simulation results are compared with standard HSPICE and reported in sections IV. Conclusions and future scope appear at the end.

2. Analysis of RLC Interconnect

The solution of interconnects are described by telegrapher's equations as

$$\frac{\partial}{\partial x}V(z,s) = -(R+sL)I(z,s)$$

$$\frac{\partial}{\partial x}I(z,s) = -sCV(z,s)$$

$$(1)$$

where 's' is the Laplace-transform variable, z is a variable which represents position; $V(z,s)$ and $I(z,s)$ stand for the voltage and current vectors of the transmission line, respectively, in the frequency domain; and R, L and C are the per unit length (p.u.l.) resistance, inductance, and capacitance matrices, respectively.

The solution of (1) can be written as an exponential matrix function as

$$\begin{bmatrix} V(d,s) \\ -I(d,s) \end{bmatrix} = e^{\phi d}\begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix}$$

$$(2)$$

where

$$\phi = \begin{bmatrix} 0 & -Z \\ -Y & 0 \end{bmatrix}$$

and 'd' is the length of the transmission line, with Z=R+sL and Y=sC. The exponential matrix of (2) can be written in terms of cosh and sinh functions as

$$e^{\phi d} = \begin{bmatrix} \cosh\left(d\sqrt{ZY}\right) & -Y_0^{-1}\sinh\left(d\sqrt{YZ}\right) \\ -Y_0\sinh\left(d\sqrt{YZ}\right) & \cosh\left(d\sqrt{YZ}\right) \end{bmatrix}$$

where

$$Y_0 = Y(\sqrt{YZ})^{-1}$$

Equation (2) does not have a direct representation in the time domain, so it is difficult to analytically predict the delay and overshoot of transmission lines.

3. Proposed Umodel

This model is based on a generalized U-transform [14]. For the power series expansion of a function f(x), where 'x' is a complex variable

$$f(x) = \sum_{n=0}^{\infty} a_n x^n$$

The sequence $\{s_n\}$ is a partial sum of original series

$$s_n = \sum_{k=0}^{n-1} a_k x^k$$

The closed form rational function approximation for an exponential matrix is

$$u_{kn}(\{S_n\}) = \frac{\sum_{j=0}^{n+k-1} x^i \sum_{j=0}^{k} w_{knj} a_{j-i}}{\sum_{j=0}^{k} w_{knj} x^i}$$

$$(3)$$

where

$$w_{knj} = (-1)^j \frac{k!}{j!(k-j)!}\frac{(n+k-j)^{k-2}}{a_{n+k-j-1}}$$

$$(4)$$

Thus u_{kn} represents a table of rational functions, each element of which is obtained from n + k terms of the original sequence $\{S_n, n = 1, 2,...\}$ and is an approximant of the function f(x) specified above.

Calculation procedure for estimating delay and overshoot using U-approximants are as follows.

(i) Use the Interconnect line parameters as per Table I.
(ii) Telegrapher's equations are solved and the solution can be written as exponential matrix.
(iii) This transfer function matrix parameters can be approximated using the U-model.
(iv) In the proposed model calculate the coefficient of the exponential function i.e., a_i where

$$0 \le i \le n$$

(v) Calculate w_{knj} from the relation (4)
(vi) Calculate the inner sum of the Eq (3) numerator.
(vii) Total sum of the numerator is obtained
(viii) Calculate the total sum of the denominator of the U-approximants
(ix) Calculate the U-approximants
(x) Make use of the U-approximants to get approximated transfer function
(xi) Find the time domain response of approximated transfer function using inverse Laplace transform to estimate delay and overshoot of interconnect.

The basic idea of the matrix rational-approximation model is to use predetermined coefficients to analytically obtain rational functions for (2). To obtain a passive model, the exponential function $e^{\phi d}$ is approximated using Eq (3) and the resultant model is used for obtaining time response.

A single RLC line is shown in Fig. 1. The line is driven by a step input and 1-V finite ramp with rise time of 0.1 ns. This represents a point-to-point interconnection driven by a transistor (modelled as a resistance R_s) and connected to the next gate (modelled as a capacitance C_l).
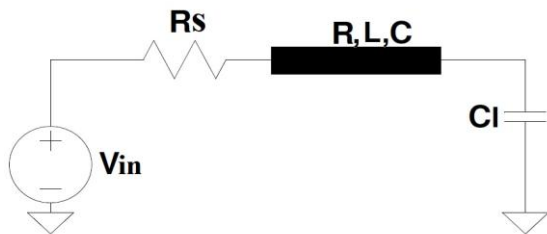
Fig. 1. Circuit model of the single-line distributed RLC interconnect.

The frequency-domain solution at the far end is expressed as

$$V_f = \frac{V_{in}}{(1 + sR_sC_l)\cosh(\Gamma d) + (R_sY_0 + sC_lY_0^{-1})\sinh(\Gamma d)}$$

(4)

where

$$\Gamma = \sqrt{YZ} \, ,$$

R_s is the source resistance at the near end, C_l is the load capacitance at the far end, and V_{in} is the input voltage. The exact transfer function of distributed RLC transmission line has cosh and sinh terms, which are multiplied with Y_o and it's inverse. It is extremely difficult to find the time domain response of this complex transfer function, so several approximations are proposed in literature to find the time domain response. An approximate transfer function has been derived using U-transform. This transfer function is inverse Laplace transformed to get time domain response for estimation of delay and overshoot in single RLC interconnect.

4. Simulation Results

The single RLC line is presented in this section to demonstrate the validity and efficiency of the proposed method. The results were obtained using MATLAB R2010a operating on HP 64-bit Intel i5 processor with clock speed of 2.53 GHz and are also compared with HSPICE using the W-element method.

The typical interconnect parameters [13] considered for simulation of single RLC interconnect are given in table-I. The Pade approximation, Eudes model and proposed U-approximation are implemented in MATLAB for the same set of input parameters and various approximation orders.

Table I: The values of Interconnects parameters [13]

Vdd	1v
Length	0.2cm
Resistance	88.29Ω/cm
Capacitance	1.8pF/cm
Inductance	15.38nH/cm
Load capacitance	0.05fF to 0.1fF
Source resistance	20Ω to 100Ω
Input ramp rise time	0.1ns

The accuracy of proposed model validated using the frequency response of cosh function as shown in Fig. 2. The frequency response is obtained using pade (3/3) and proposed U-model (3/3) are compared with the exact solution of telegrapher's equations. It is observed that, the proposed method is better than Pade method and well matches with exact cosh function for the order of 3/3 up to the frequency of 25 GHz.

The far-end responses to a finite ramp input of single interconnect is plotted in Fig. 3. The plots compared the responses of proposed, Pade and HSPICE W-element models.
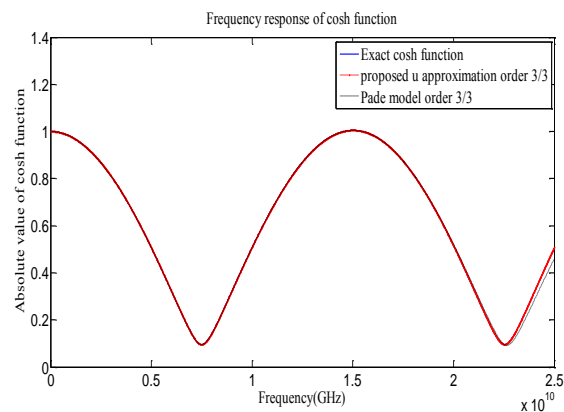

Fig: 2. Frequency response of exact cosh function, proposed U-approximation order 3/3 and Pade approximation order 3/3.

From Fig. 3, it is noticed that, the proposed U-approximation and Pade method are very close as compared to HSPICE. But Eudes model of order 4 has more overshoot as compared to other methods.
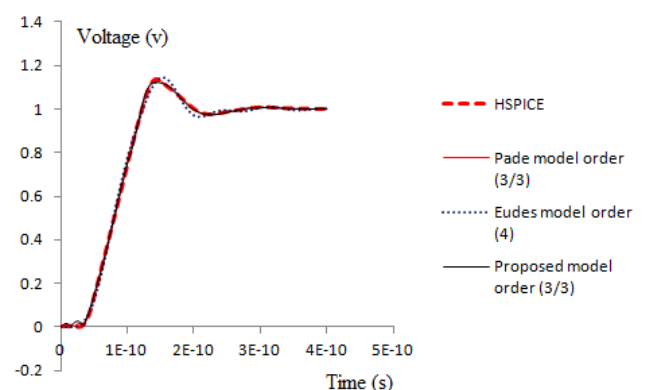

Fig: 3.Transient analysis of single interconnect line, when length =0.2cm, R_s=50Ω and C_l=50fF.

The MATLAB results of step response and finite ramp response are plotted for the line length of 0.2 cm, source resistance of 100Ω and load capacitance of 100fF. Step response in Fig. 4 has less ringing in proposed method as compared to Pade method, for the same approximation order of 3/3, whereas Fig. 5 gives finite ramp response of single line interconnect using U-model matches very well with the

HSPICE. But Eudes model needs more settling time as compared to the proposed model.
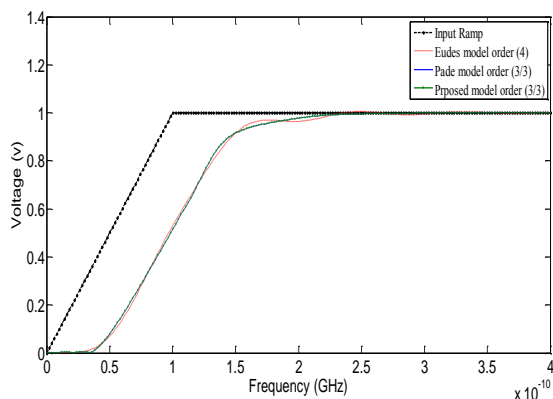

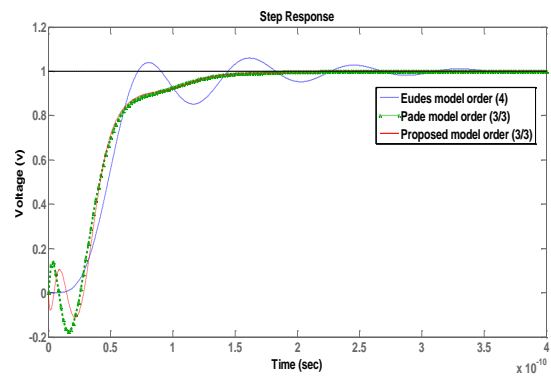Fig: 4.Step response of single line when length =0.2cm, Rs=100Ω and Cl=100fF.

Fig: 5.Ramp response of single line when length =0.2cm, R_s=100Ω, C_l=100fF.

Table II: Comparisons of 50% delay of HSPICE W Element, Eudes model Pade model and proposed model for various lengths, source Resistances and load Capacitances.

L (cm)	Rs (Ω)	Cl (fF)	HSPICE	Eudes model order (4)	Pade model order 3/3	Proposed Model order (3/3)
			50% delay (ps)	50% delay (ps) (%Error)	50% delay (ps) (%Error)	50% delay (ps) (%Error)
0.2	50	50	79.8	79.1 (0.8%)	80.2 (0.5%)	80.2 (0.5%)
	100	100	98.7	96.8 (1.92%)	98.6 (.1%)	98.65 (0.05%)
0.5	50	50	135.7	142.8 (5.23%)	137.8 (1.54%)	137.7 (1.4%)
	100	100	156.6	162.6 (3.83%)	151.9 (3%)	155.3 (0.83%)
1.0	50	50	231.2	250.2 (8.21%)	211.1 (8.69%)	224.7 (2.811%)
	100	100	255.6	284.8 (11.42%)	249.7 (2.3%)	252.5 (1.21%)

Table III: Comparisons of overshoot of HSPICE W Element, Eudes model, Pade model and proposed model for various lengths, source Resistances and load Capacitances.

L (cm)	Rs (Ω)	Cl (fF)	HSPICE	Eudes model order (4)	Pade Order 3/3	Proposed Model order (3/3)
			Overshoot (V)	Overshoot (V) (%Error)	Overshoot (V) (%Error)	Overshoot (V) (%Error)
0.2	50	50	1.14	1.14 (0%)	1.12 (1.7%)	1.13 (0.87%)
	100	100	1.00	1.00 (0%)	1.00 (0%)	1.00 (0%)
0.5	50	50	1.15	1.24 (7.8%)	1.15 (0%)	1.14 (0.87%)
	100	100	1.00	1.03 (3%)	1.00 (0%)	1.00 (0%)
1.0	50	50	1.00	1.09 (9%)	1.02 (2%)	1.01 (1%)
	100	100	1.00	1.00 (0%)	1.00 (0%)	1.00 (0%)

The Tables II and III give the comparisons of 50% delay and overshoot values obtained using HSPICE for various lengths, source Resistances and load Capacitances. These tables include the percentage error values with respect to HSPICE. From Table II the Eudes model of order 4 has worst case error of 11.42%, whereas Pade and proposed models have 8.69% and 2.811%.

It can be observed that the methods implemented for global lines have more error percentage than our proposed method. Both Pade and proposed methods perform similarly for smaller length interconnects while Eudes method has more error percentage.

As noticed in Table III, the Eudes model has worst case overshoot error percentage of 9%, but Pade model has an error percentage up to 2% while the proposed model has error within 1%. In the case of overshoot estimation our model is best for all cases. For 2 mm range lines the proposed method has delay and overshoot errors within 1% .

5. Conclusion

This paper presents a U-transform based closed form model for delay and overshoot estimation of high speed VLSI interconnects in DSM regime. A single line interconnect has been used for validating the proposed model by comparing with the Eudes model, Pade method and HSPICE. In SOC (system on chip) applications, for global lines of lengths 2 mm and above the proposed method is found to be more accurate than existing methods. This method can be used to estimate the signal integrity characteristics of Carbon nano tubes.

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